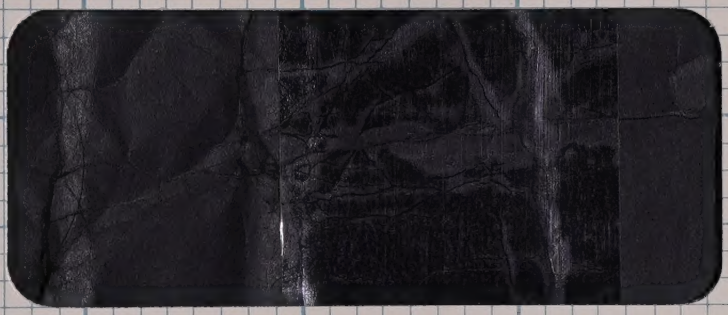

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WATKINS-JOHNSON

MICROFICHED

INSTRUCTION MANUAL

FOR THE

IFD121 AND IFD 121-1 IF DEMODULATORS

MICROFICHED

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WATKINS-JOHNSON COMPANY
700 Quince Orchard Road
Gaithersburg, MD 20878

April 1987

WARNING

This equipment employs dangerous voltages which may be fatal if contacted. Exercise extreme caution in working with this equipment with any of the protective covers removed.

IFD121-1 IF DEMODULATOR

1.0 INTRODUCTION

The IFD121-1 IF Demodulator is mechanically and electrically identical to the IFD121 IF Demodulator except for the expanded capability to install customer selectable bandwidths in the IFD121-1 that are not part of the IFD121 IF Demodulator.

2.0 ELECTRICAL/MECHANICAL CHARACTERISTICS

While the IFD121 IF Demodulator is designed for fixed bandwidths of 150 kHz, 500 kHz, 1 MHz, and 4 MHz, the IFD121-1 is only limited to four installed bandwidths, that range from 2.85 kHz through 4 MHz.

Operating procedures and all other information contained in the following sections of the IFD121 INSTRUCTION MANUAL apply equally to the IFD121 Demodulator and the IFD121-1 Demodulator.

Available, customer selectable IF bandwidths for the IFD121-1 are shown on the following page.

The following WJ-9928-XXXX IF Bandwidths may be installed in the IFD121-1 IF Motherboard A1A5A1 through A1A5A4 slots:

AVAILABLE BANDWIDTHS	WJ-9928-XXX PART NUMBER
2.85 kHz	371155-3
4 kHz	371155-4
5 kHz	371155-6
7 kHz	371155-5
10 kHz	371155-1
20 kHz	371155-2
50 kHz	371156-1
80 kHz	371156-5
100 kHz	371156-2
150 kHz	371156-4
200 kHz	371156-3
250 kHz	371158-11
300 kHz	371158-4
420 kHz	371158-10
500 kHz	371158-5
700 kHz	371158-7
1 MHz	371158-1
1.4 MHz	371158-8
2 MHz	371158-2
2.8 MHz	371158-9
4 MHz	371158-3

INSTRUCTION MANUAL

FOR

IFD121 IF DEMODULATOR

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1/86

WARNING

This equipment employs dangerous voltages which may be fatal if contacted. Exercise extreme caution in working with the equipment with any of the protective covers removed.

EQUIPMENT AND PROCEDURAL SAFETY

Equipment and procedural safety practices are paramount to both the user and manufacturer of this equipment. As a result, the following general guidelines are presented as a reminder to prevent possible injury and equipment damage.

1. Preventive and corrective maintenance on this equipment, with the protective covers removed and power applied, should be performed by skilled technicians familiar with this equipment.

2. With equipment power off and with the equipment power cord disconnected from a power source, there is a possibilty that capacitors in the equipment may still be charged.

3. Replace defective equipment power fuses with fuses of the same size and type which are both specified on the equipment and in this publication.

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SECTION I

GENERAL DESCRIPTION

1.1 ELECTRICAL CHARACTERISTICS

The IFD121 IF Demodulator (Figure 1-1) provides Intermediate Frequency signal demodulation capabilities for any receiver or RF tuner which has a 21.4 MHz low level IF or SM output. The demodulator is compatible with the WJ-9040 Receiving System Family and shares the WJ-9040 System characteristics of low power consumption, modular construction and high performance.

The IFD121 can demodulate AM, FM, CW, and pulsed signals and can be operated in both a local and remote control mode. Four selectable IF bandwidths are available at 150 kHz, 500 kHz, 1 MHz, and 4 MHz. Output gain can be controlled either manually via front panel adjustment or automatically via Automatic Gain Control (AGC) circuits.

1.2 MECHANICAL CHARACTERISTICS

The demodulator normally is mounted in a 19 inch WJ-9040 System Equipment Frame (EFR100) and occupies one quarter of the width of the frame. The front panel is a 0.19 thick aluminum plate overlaid with a 0.032 thick black bezel etched with control markings. The front panel is mounted to two nickel plated brass modules which make up the main frame. All operating controls and indicators are located on the front panel, while input and output lines are located on the rear of the two modules.

A 25 pin D type connector engages the back plane of the EFR100 equipment frame interfacing the required control I/O, DC supply voltages, and Polled I/O signals. Ten SMA coaxial connectors interface the 21.4 MHz input, 21.4 MHz output, two FM Video outputs, two AM Video outputs, two 21.4 MHz Wideband IF outputs, Selected Audio outputs, and Signal Strength output.

1.3 OPERATIONAL OVERVIEW

The following paragraph describes the WJ-9040 operational environment in terms of its interaction with the IFD121 IF Demodulator.

1.3.1 BASIC SYSTEM ORGANIZATION

The IFD121 IF Demodulator is part of the WJ-9040 Receiving System Family And will typically be operated in a WJ-9040 System environment. The demodulator is designed to plug into the WJ-9040 EFR100 Equipment Frame. This frame defines the interface point between the demodulator and the WJ-9040 system. The demodulator receives all DC power, control instruction and commands via a 25 pin D type connector that mates with a counterpart on the equipment frame. The WJ-9040 System Receiver is designed to communicate with the demodulator from two primary sources: from a WJ-9040 System Receiver Controller or from an external control via RS-232 / IEEE-488. Both sources

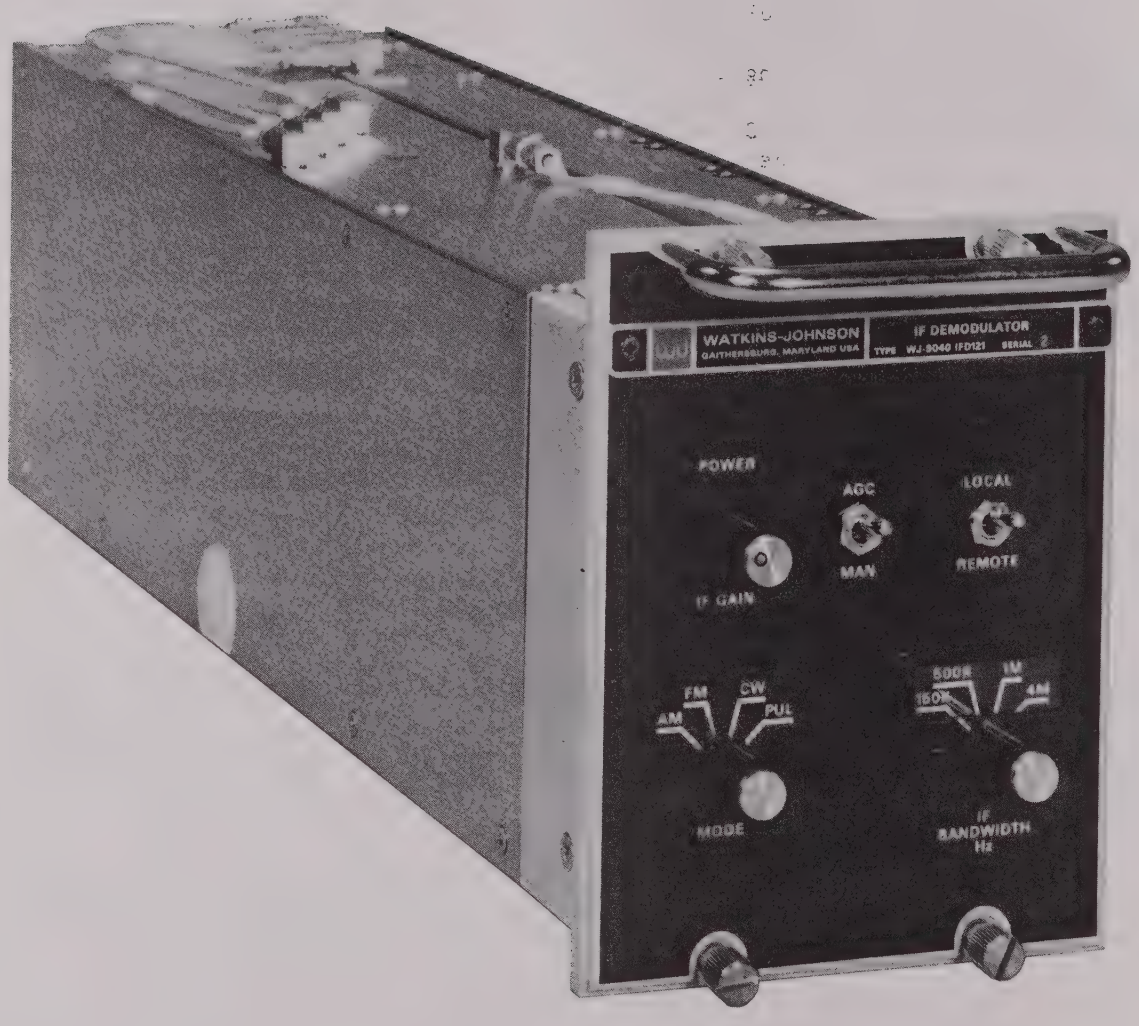


Figure 1-1. IFD121 IF Demodulator

interface with the demodulator through the IOM108 I/O Control Module on the equipment frame. Actual communication with the demodulator occurs via a 72-bit serial data stream connecting the IOM108 and the demodulator. Figure 1-2 is a simplified block diagram showing the relationship between the major elements in the WJ-9040 System.

1.3.2 EQUIPMENT SUPPLIED

The following items are supplied with the IFD121:

- IFD121 IF Demodulator
- IFD121 Instruction Manual

1.3.3 EQUIPMENT REQUIRED BUT NOT SUPPLIED

The following items comprise the minimum complement necessary to effectively use the demodulator as a component in a WJ-9040 receiving system:

- EFR100 Equipment Frame
- EPS100 Power Supply
- IOM108 I/O Control Module with D10488 or D10232 Board for remote control via IEEE-488 or RS-232 bus.

1.4 EQUIPMENT SPECIFICATIONS

See Table 1-1 for IFD121 IF Demodulator specifications.

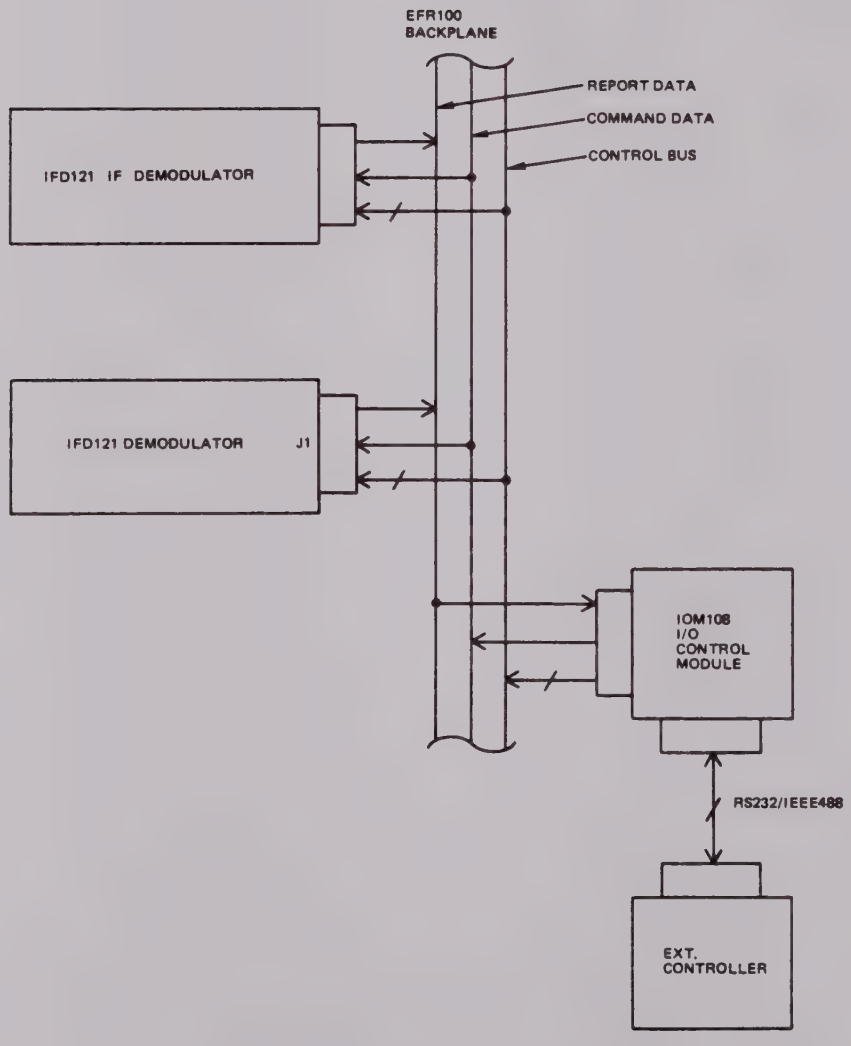


Figure 1-2. WJ-9040 System Configuration

Table 1-1. IFD-121 IF Demodulator Specifications

Input Frequency	21.4 MHz
Input Impedance	50 ohms, unbalanced, nominal
IF Bandwidths	150 kHz, 500 kHz, 1 MHz and 4 MHz
IF Shape Factor	IF BW 60 dB/3 dB, typical 150 kHz 3.5 500 kHz 3.5 1 MHz 4.0 4 MHz 4.0
Detection Modes	AM, FM, CW and PULSE
Noise Figure	16 dB maximum
Dynamic Range	Demodulator meets performance specifications over the following range of input levels; 150 kHz BW -98 to -38 dBm 500 kHz BW -93 to -38 dBm 1 MHz BW -90 to -30 dBm 4 MHz BW -84 to -24 dBm
AGC Threshold	150 kHz -88 dBm 500 kHz -83 dBm 1 MHz -80 dBm 4 MHz -74 dBm
IF Gain Control	Manual Gain Control AGC Pulse peak power leveling (PULSE) AGC average power leveling (non-PULSE)
Manual Gain Control Range	60 dBm minimum
Pulse Peak Power Leveling	Pulsewidth = 1 μsec minimum, PRR=100 pps minimum
Leveling	Output range variation less than ±1 dB
Control Range	50 dB minimum
Recovery Time	After a 250 millisecond no signal interval, gain increases at 3 dB/millisecond.
Setting Time	For +5 dB step, output settles within 1 dB of final value within 100 millisecond.
Average Power Leveling	
Leveling	Output range variation less than ±1 dB
Control Range	50 dB minimum
Settling Time	For ±5 dB step, the output settles within 1 dB of final value within 100 milliseconds.
FM Video (2)	1 Vpp into 75 ohms for peak frequency deviation equal to one half of selected IF BW. Available in all modes.
AM Video (2)	1 Vpp into 75 ohms with input level equivalent to AGC threshold and 50% AM.
21.4 MHz Wideband IF Output	10 dB above IF input level. 50 ohms, 10 MHz bandwidth.
Selected Audio Output	1.25 Vrms into 600 ohms, nominal at AGC threshold and 50% AM.
Signal Strength Output	0 to +10 Vdc into 10 K ohms

Table 1-1. IFD121 Demodulator Specifications (Cont'd)

Differential Gain	The AM video output shall change less than 2 dB for a 50% modulated input signal modulated between 10 Hz and 20 Hz rates.
Differential Phase	15 degrees maximum phase shift change between IF input and video output when input signal is modulated between 10 Hz and 20 Hz rates and up to 100% modulation. ± 10 degrees maximum phase shift change for a modulation frequency of 10 Hz when input level is varied over the control dynamic range.
Digital Control	72 bit serial word (WJ-9040 compatible)
Environmental Conditions:	
Temperature, Operating	0° to +50° C
Temperature, Non-operating	-40° to +70° C
Size: Height	5.2 inches (132 mm)
Width	4.0 inches (102 mm)
Depth	14.38 inches(356 mm)
Weight	9 lbs (4 kg)
Power Consumption	9 watts, maximum

SECTION II

INSTALLATION AND OPERATION

2.1 UNPACKING AND INSPECTION

Examine the shipping carton for damage prior to unpacking equipment. If the carton appears to be damaged, have the carrier's agent present when the equipment is unpacked. If this is not possible, retain all packaging material and shipping containers for the carrier's inspection to verify damage to the equipment after unpacking. Also verify that the equipment shipped corresponds to the packing slip. Contact the Watkins - Johnson Company, CEI Division, or your Watkins - Johnson representative for any discrepancies or shortages.

The unit was thoroughly inspected and factory adjusted for optimum performance prior to shipment. It is therefore ready for use upon receipt. After uncrating and checking contents against the packing slip, visually inspect all exterior surfaces for dents and scratches. If external damage is visible, remove the dust covers and inspect the internal components for apparent damage. Then check the internal cables for loose connections and plug-in items such as printed wiring boards which may have been loosened from their receptacles.

2.2 REPACKING

If the equipment must be prepared for reshipment, the packing methods should follow the pattern established in the original shipment. If retained, the original materials can be reused or at least provide guidance for the repackaging effort. Conditions during storage and shipment should be limited as follows:

Maximum humidity: 95% (no condensation)

Temperature Range: -40°C to 70°C

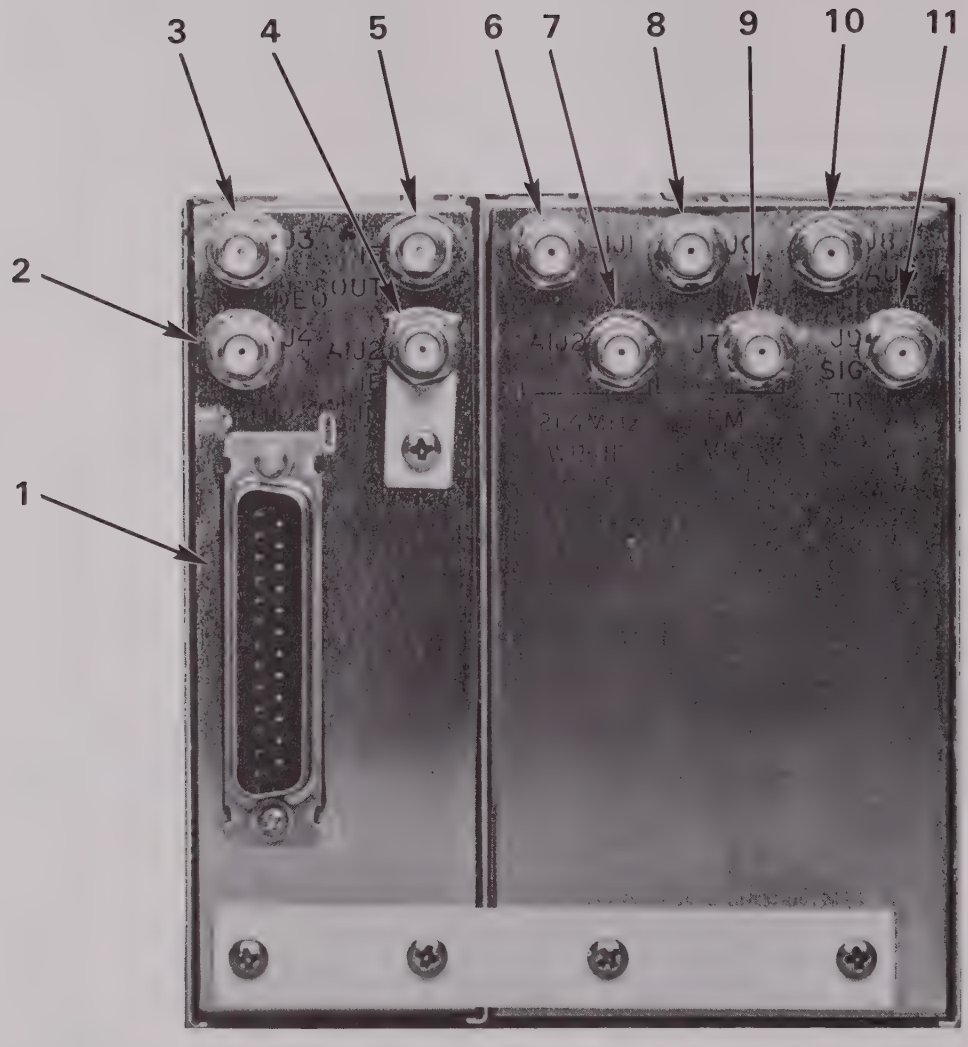
2.3 INSTALLATION PROCEDURES

THE IFD121 IF Demodulator is designed to mount in the EFR100 Equipment Frame. Specific installation procedures for the EFR100 are covered in the WJ-9040 EFR100 Operator's Manual. However, the following general guidelines should be observed when using the demodulator in the WJ-9040 Operational Environment:

1. Operating temperature range should be from 0°C to +50°C.

2. Free air circulation should be allowed between equipment frames. Multiple stacking significantly increases ambient temperatures.

3. Use only stable, properly grounded AC power for the WJ-9040 equipment.



1. Power/Command Control J1
2. AM Video Out J4
3. AM Video Out J3
4. IF In J10
5. IF Out A2J4
6. 21.4 MHz WB IF Out A1J1
7. 21.4 MHz WB IF Out A1J2
8. FM Video Out J6
9. FM Video Out J7
10. Audio Out J8
11. Signal Strength Out J9

Figure 2-1. IFD121 IF Demodulator Input/Output Connectors

2.4 IF DEMODULATOR OPERATION

The following paragraphs constitute a guide designed to familiarize the operator with the different operating functions available with the demodulator. The functions and uses of the front panel controls and indicators are explained and demodulator operating instructions are provided. It is recommended that paragraph 1.3, Operational Overview, be studied before attempting to operate the demodulator.

2.4.1 INTRODUCTION

The IFD121 IF Demodulator incorporates the following operational features:

- Remote control capability through the IOM108 interface
- Automatic or manual gain control
- Detection of AM, FM, CW, or pulsed signals

2.4.2 CONTROLS AND INDICATORS

The funtions and uses of the front panel controls and indicators are explained in the following paragraphs. Refer to Figure 2-2 for the location of the front panel controls and indicators.

2.4.2.1 AGC/Manual Gain Control Switch

This switch selects either automatic or manual gain control operation.

2.4.2.2 Local/Remote Switch

This switch selects either local or remote control operation. In local control, remote access is locked out.

2.4.2.3 IF Bandwidth Select Switch

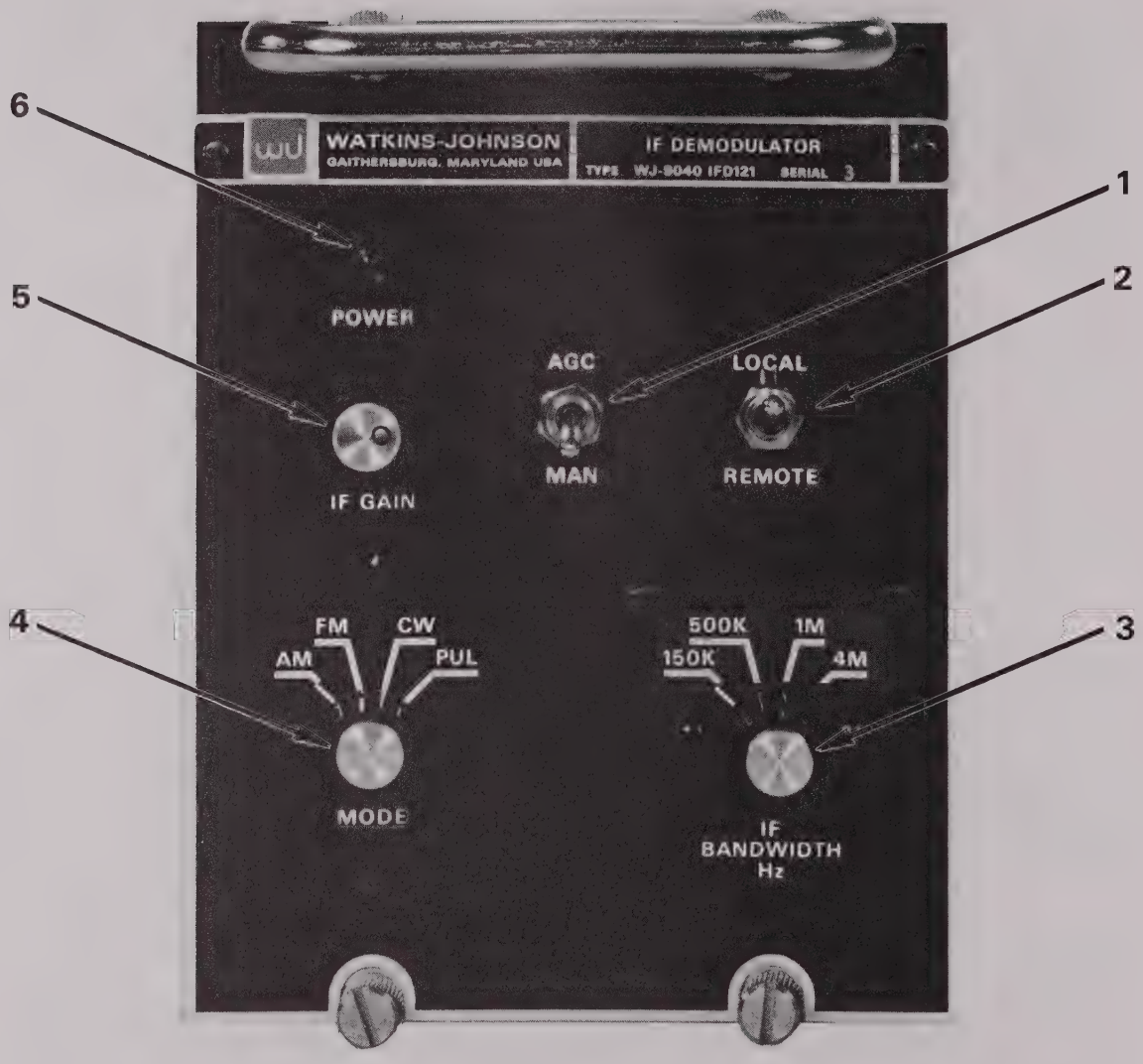
This switch provides the capability to select four different IF bandwidths: 150 kHz, 500 kHz, 1 MHz, or 4 MHz.

2.4.2.4 Mode Select Switch

This switch provides the capability to select the detection of four IF signal types: AM, FM, CW, or Pulse.

2.4.2.5 IF Gain Control

This control provides the capability to adjust the gain level of the IF signal when the AGC/MAN switch is in the MAN position. The AGC/MAN switch is explained in paragraph 2.4.2.1.



1. AGC/Manual Gain Control Switch
2. Local/Remote Switch
3. IF Bandwidth Select Switch
4. Mode Select Switch
5. IF Gain Control
6. Power Light

Figure 2-2. Front Panel Controls and Indicators

2.4.2.6 Power Light

When illuminated, this light indicates that operating power is available to the demodulator.

2.4.3 OPERATING PROCEDURES

The following paragraphs provide the procedures required to correctly operate the demodulator. Before proceeding the operator should first become familiar with the functions of the front panel controls which are explained in paragraph 2.4.2.

2.4.3.1 Local Control Mode

When the LOCAL/REMOTE switch is in the LOCAL position, the operator has the capability to control the demodulator from the front panel controls. The operator can select gain mode, detection mode and IF bandwidth via front panel controls.

2.4.3.1.1 AGC Gain Mode

When the AGC/MAN switch is in the AGC position, the gain of the demodulator is automatically controlled by the internal circuits. The IF GAIN control is inoperative.

2.4.3.1.2 Manual Gain Mode

When the AGC/MAN switch is in the MAN position, the IF GAIN control can be rotated clockwise or counterclockwise to adjust the IF signal level as desired. Maximum clockwise position is maximum unit gain.

2.4.3.1.3 Detection Mode

The detection mode switch permits the operator to select AM, FM, CW, or PULSE detection to match the modulation characteristics of the IF signal to the demodulator. PULSE mode is a special type of AM detection that permits satisfactory reception of extremely narrow pulse width signals. CW mode is identical to AM mode in the IFD121.

2.4.3.1.4 IF Bandwidth

The IF Bandwidth switch permits the operator to select IF bandwidths of 150 kHz, 500 kHz, 1 MHz, and 4 MHz to match the signal bandwidth of the IF signal to the demodulator.

2.4.3.2 Remote Control Mode

When the LOCAL/REMOTE switch is in the REMOTE position, the demodulator is configured for control by an external controller. The front panel controls are disabled and selection of gain, detection mode and IF bandwidth is performed by the external controller.

Figure 2-3 shows a typical configuration for implementing remote control by an ASCII type computer terminal. As shown, the minimum equipment configuration consists of a computer terminal equipped for either IEEE-488 or RS-232 communication, an EFR100 equipment frame, an IOM108 interface module equipped for either IEEE-488 or RS-232 communication, and an IFD121 IF Demodulator. Using English-like ASCII commands, the controller communicates directly with the IOM108 which decodes the commands and communicates with the demodulator via the command/report data lines on rear panel J1. Additionally, the demodulator reports signal strength data to the controller via the polled I/O lines on rear panel J1 through the IOM108. Table 2-1 contains a list of specific commands which may be sent to the IFD121 IF Demodulator from the controller via the IOM108. Detailed information for implementing remote control via RS-232 or IEEE-488 may be found in the WJ-9040 IOM108 Operator's Manual.

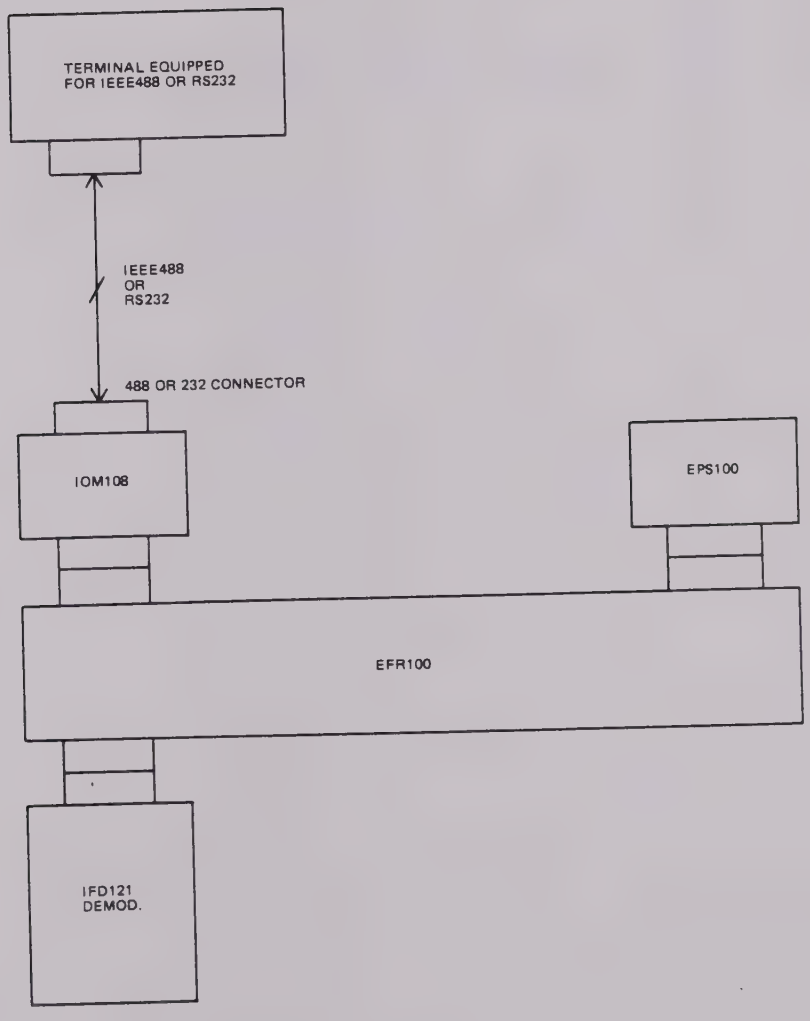


Figure 2-3. Remote Control Hardware Configuration

Table 2-1. IFD-121 Demodulator Remote Commands

COMMAND	DESCRIPTION	EXAMPLE
AFC	Turns on automatic freq. control	AFC
AFC/	Turns off aut. freq. control	AFC/
AFC?	Asks for AFC state	AFC?
AGC	Turns on automatic gain control	AGC
AGC/	Turns off auto. gain control	AGC/
AGC?	Asks for AGC state	AGC?
AM	Selects AM detection mode	AM
BW n	Selects bandwidth 1 to 4	BW 2
BW?	Asks for bandwidth #	BW?
BWC?	Asks for bandwidth in kHz or MHz	BWC?
CLR	Resets demodulator	CLR
CW	Selects CW detection mode (same as AM mode)	CW
DET?	Asks for the detection mode	DET?
EXAM n	Asks for the slot status 1 <= n ,= 8	EXAM 3
FM	Selects FM detection mode	FM
PLS	Selects Pulse detection mode	PLS
RFG n	Sets RF gain level 0<= n < 64 (64 = minimum gain)	RFG 40
RFG?	Asks for the RF gain level	RFG?
RMT	Puts the IFD into remote mode	RMT
SLOT n	Addresses a specified slot in frame	SLOT 7
SS?	Asks for signal strength	SS?

SECTION III

CIRCUIT DESCRIPTION

3.1 INTRODUCTION

This section describes the theory of operation of the demodulator. A simplified block diagram is provided to show overall functional partitioning of the demodulator. Functional block diagrams are provided for each of the demodulator's major sections to show functional signal flow through the demodulator. The functional descriptions are followed by individual circuit-level descriptions of each demodulator module.

3.2 GENERAL DESCRIPTION

Figure 3-1 is a simplified block diagram of the demodulator. The demodulator functions have been grouped into two sections:

a. IF Processing Section

b. Digital Control Section

A general discussion of each section follows.

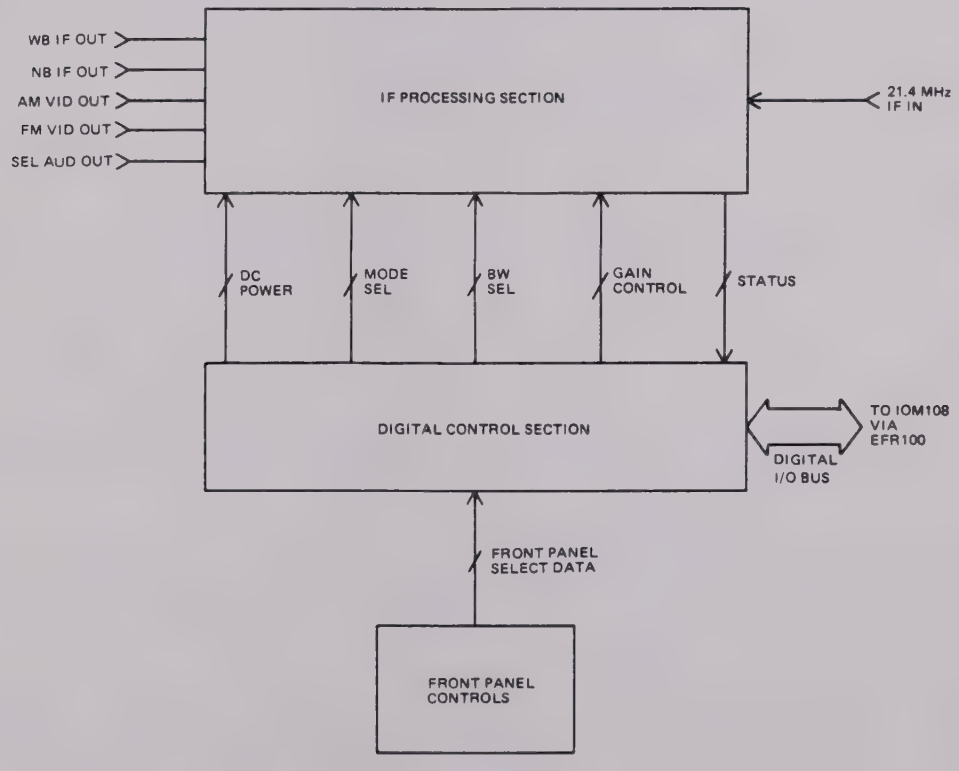


Figure 3-1. IFD121 Demodulator Simplified Block Diagram

3.2.1 IF PROCESSING SECTION

A general description of the IF Processing Section functions and signal interfaces is provided in the following paragraphs.

3.2.1.1 IF Processing Section Functions

The IF Processing Section performs the following functions:

a. Band Limiting - The 21.4 MHz IF signal is routed through one of four selectable bandpass filters. Available bandwidths range from 150 kHz to 4 MHz.

b. IF Signal Amplification - A combination of broadband and tuned high-gain IF amplifier stages established the overall gain of the demodulator.

c. Gain Control - An AGC amplifier adjusts the overall demodulator gain under conditions of varying input signal levels in the AGC mode. In manual mode the operator adjusts the gain with front panel control.

d. Signal Demodulation -Two signal demodulators provide demodulator AM, FM, CW and pulsed video outputs. In the IFD121 the CW mode is the same as the AM mode.

3.2.1.2 Input / Output Signal Interfaces

The following input/output signals interface with the IF Processing Section:

a. 21.4 MHz IF in - A 21.4 MHz IF signal input from an external source serves as the main signal input to the demodulator. Input impedance is 50 ohms.

b. Mode Select - The Digital Control Section sends a data word to select AM, FM, CW or pulse modes of operation.

c. Bandwidth Select - The Digital Control Section sends a data word to select each of the four IF filters and one of four FM demodulators.

d. Gain Control - The Digital Control Section sends a data word to select either automatic or manual gain modes and a variable manual gain voltage to adjust the gain of the demodulator in manual mode.

e. DC Power - The Digital Control Section sends DC voltage of +/-18 Vdc and +8 Vdc to power the circuitry in the IF Processing Section. These voltages are later regulated to +/-15 Vdc and +5Vdc.

f. Wideband IF Output - A low level wideband 21.4 MHz IF signal is provided to drive a Spectrum Analyzer or similar monitoring equipment. The impedance is 50 ohms and the signal bandwidth is 10 MHz. Nominal output level is 10dB above the input signal.

g. Narrowband IF Output - This is a high level 21.4 MHz IF output signal that is band limited to the selected bandwidth of the demodulator. Output impedance is 50 ohms. Nominal output level is -20dBm at AGC threshold.

h. AM Video Output (two) - A demodulator AM output signal is provided as a rear panel demodulator output. This output is 75 ohms, with a bandwidth equal to one-half of the selected IF bandwidth, and is nominally one volt peak-to-peak or greater in signal level with 50% AM and input signal level equal to AGC threshold.

j. FM Video Output (two) - A demodulated FM output signal is provided as a rear panel demodulator output. This output is 75 ohms, with a bandwidth equal to one-half of the selected IF bandwidth, and is nominally 0.6 volt peak-to-peak with peak deviation equal to one third of the selected IF bandwidth and input signal level above AGC threshold.

k. Status - These DC outputs are sent to the Digital Control Section and represent the signal strength voltage, AFC, and the actual IF bandwidth selected at the front panel.

3.2.2 DIGITAL CONTROL SECTION

A general description of the Digital Control Section functions and signal interfaces are provided in the following paragraphs.

3.2.2.1 Digital Control Section Functions

The Digital Control Section performs the following functions:

a. Demodulator Control - The Digital Control Section generates the digital control words necessary to operate the IF Processing Section of the demodulator.

b. Front Panel Interface - Operator selected parameter inputs are interfaced from the front panel to the digital circuitry to generate demodulator digital control words.

c. External Controller Interface - External controller commands are interfaced with the digital circuitry to produce demodulator digital control words. The Digital Control Section also sends demodulator status words to the external controller through the IOM108.

3.2.2.2 Input / Output Signal Interfaces

The following input/output signals interface with the Digital Control Section:

a. Front Panel Select Data - Select data is entered from the front panel control to the Digital Control Section to permit operator selection of demodulator operating parameters.

b. Digital I/O Bus - The data control bus interfaces between the Digital Control Section and the rear panel I/O connector. This bus permits an external control device to send parameter data to the demodulator. The bus also sends status and parameter information from the demodulator to other demodulator units.

c. Mode Select - The Digital Control Section sends mode select data to the IF Processing Section to select AM, FM, CW or Pulse modes.

d. Bandwidth Select Data - The Digital Control Section sends a bandwidth select data word to the IF Processing Section to select one of the four available IF bandwidths.

e. Gain Control - The Digital Control Section sends a gain select word to the IF Processing Section to select manual or automatic gain modes. A variable manual gain voltage is also sent to permit manual gain adjustment of the IF Processing Section.

f. Polled I/O - DC voltages are sent from the Digital Control Section to the to the IOM108 to represent the status of signal strength and read request.

g. DC Power - The Digital Control Section sends dc voltages of +/-18 and +8 Vdc to the IF Processing Section.

3.3 THEORY OF OPERATION

The following paragraghs provide a detailed circuit description of each of the demodulator modules. Simplified block diagrams are used throughout the text to clarify the description. These block diagrams should be used in conjunction with the schematic diagrams in Section VI.

3.3.1 IF PROCESSING SECTION

Refer to Figure 3-2, IF Processing Section Block Diagram, as an aid to understand the following description. As shown in Figure 3-2, the IF Processing Section consists of the following major assemblies:

a. 21.4 MHz Bandpass Amplifier, A1A1

b. AM/SSB/CW Demodulator, A1A2

c. Video/Audio, A1A3

d. FM Demodulator Motherboard, A1A5

e. Wideband IF Assembly, A2

The IF Processing Section is the main signal processing portion of the demodulator. Signals of 21.4 MHz are amplified and band limited by module A1A1. The band limited IF signals are demodulated by modules A1A2 and A1A5 to provide AM, FM, CW or pulse video outputs.

The demodulated video outputs are amplified by A1A3 and distributed to the rear panel as AM video, FM video, and selected audio.

The wideband IF Assembly, A2, is used to provide wideband IF to the rear panel.

3.3.1.1 21.4 MHz Bandpass Amplifier, A1A1

Refer to Figure 3-3, 21.4 MHz Bandpass Amplifier (A1A1) Block Diagram, and Figure 6-1, 21.4 MHz Bandpass Amplifier Schematic Diagram, as aids in understanding the following description. The 21.4 MHz bandpass amplifier consists of an input amplification section, a bandwidth decoder, four bandpass filters, diode switches #1 and #2, and an output amplifier. The 21.4 MHz bandpass amplifier provides for the amplification and bandwidth limiting of 21.4 MHz IF signals.

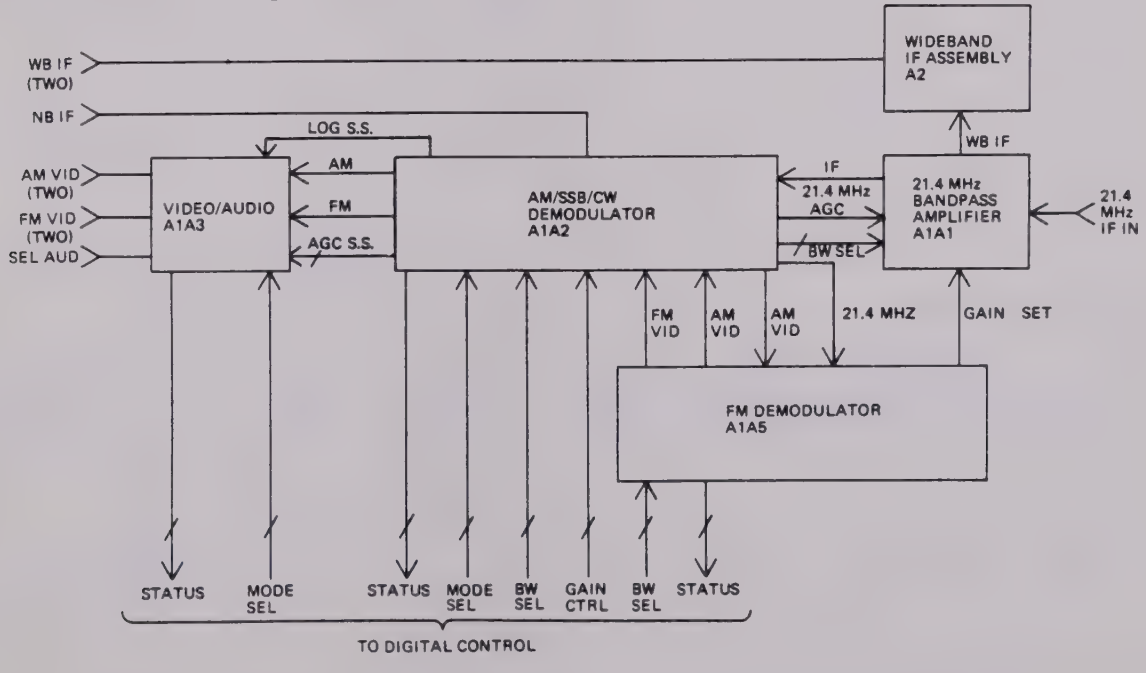


Figure 3-2. IF Processing Section Block Diagram

3.3.1.1.1 Input Amplification Section U1 through U4

IF signals of 21.4 MHz are applied to pin 2 of U1, a broadband thin film hybrid amplifier providing an overall signal gain of +12 dB. The output of U1, pin 4, drives U2, a power splitter. The power splitter provides IF outputs at pins 2 and 4. Each output has a signal loss of approximately 3.5 dB relative to the input at U2, pin 1. The pin 2 output is brought out as the wideband IF output to drive wideband IF amplifier A2A1. The pin 4 output drives U3, a WJ voltage controlled attenuator.

The attentuation of U3 is controlled by a dc voltage from A2A1 applied to U3, pin 1. U3 attenuation ranges from -2 dB for +13 Vdc input to -32 dB for +3 Vdc input. The output of U3, pin 5, drives the input of U4, pin 2. Identical to U1 is U4, a broadband thin film hybrid amplifier. The output of U4, pin 4, drives matching transformer T1, impedance matching network R1, R2, and R3, and then the input to the #1 diode switch.

3.3.1.1.2 Bandwidth Decoder U6

The bandwidth decoder, U6, is a 2-bit binary to 4-line decimal decoder. The binary input drives U6 inputs, pins 9 and 10. There are two separate 4-line decimal outputs: output 1 is sent through pins 1, 5, 2, and 4; output 2 is sent through pins 11, 15, 14, and 12.

The 2-bit binary input to U6 is driven by the bandwidth select code from module A1A2. When the input to U6 ,pins 10 and 9 is equal to 00, U6, pins 1 and 12, are at +15 Vdc. The remaining output pins are at 0 V. When the input to U6, pins 10 and 9, is equal to 10 then U6, pins 5 and 14, are at +15 V. When the inputs at pins 10 and 9 are equal to 01, pins 2 and 15 are at +15 V. When the inputs at 10 and 9 are equal to 11, pins 4 and 11 are at +15 V.

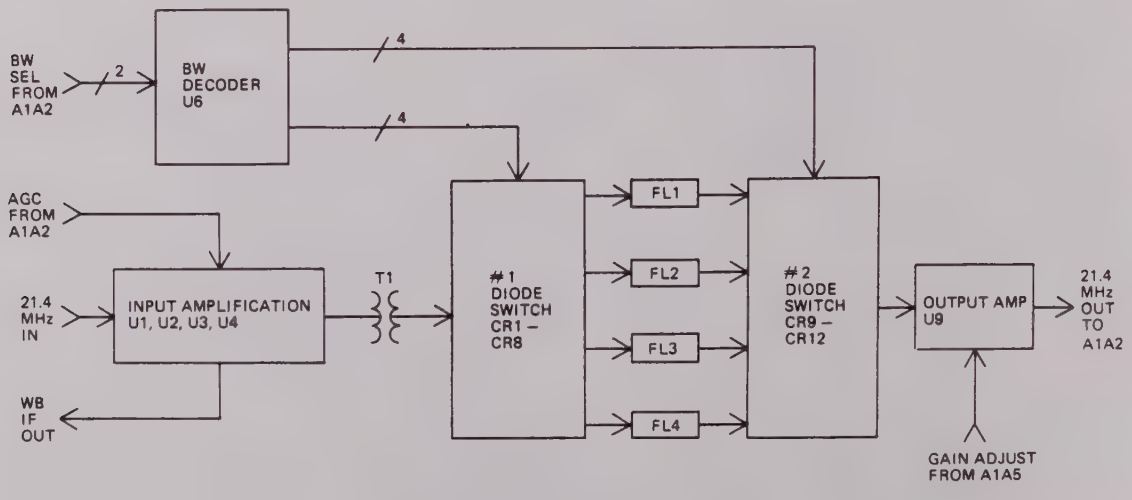


Figure 3-3. 21.4 MHz Bandpass Amplifier (A1A1) Block Diagram

Inputs		Outputs	
Pin 10	Pin 9	Pins 1,5,2,4	Pins 11,15,14,12
0	0	+15,0,0,0	0,0,0,+15
1	0	0,+15,0,0	0,0,+15,0
0	1	0,0,+15,0	0,+15,0,0
1	1	0,0,0,+15	+15,0,0,0

The decimal outputs at pins 1,5,2, and 4 provide forward bias to the #2 diode switch consisting of diodes CR9 thru CR12. The decimal outputs at pins 11, 15, 14 and 12 provide forward bias to diodes CR1, CR3, CR5, and CR7.

3.3.1.1.3 Bandpass Filters FL1 through FL4

Bandpass filters FL1 through FL4 are fixed bandpass filters with a center frequency of 21.4 MHz. The actual bandwidth of each filter is selec-Table at the customer's option. The range of bandwidths available is from a minimum of 10 kHz to a maximum of 4 MHz. The 21.4 MHz IF signal will be routed through one of the four bandpass filters by the diode switches. These filters are field-changeable to accomodate different IF bandwidths. Operation of the diodes will be explained in paragraph 3.3.1.1.4.

3.3.1.1.4 Diode Switches #1 and #2

Diode switch #1 consists of diodes CR1 through CR8. Diode switch #2 consists of diodes CR9 through CR12. These diodes exhibit low forward resistance when forward biased and extremely high resistance when reverse biased. The diodes are used to route the IF signal through one of four bandpass filters.

As an example in analyzing the operation of the diodes, the signal path through CR7, FL4, and CR12 will be discussed.

Assuming that the BW select code from A1A2 is equal to 00, the output of U6, pins 1 and 12 will equal +15 V, and the remaining output pins will equal zero volts. Diode switch #1, diode CR7, is forward biased, CR8 is reverse biased, and diode CR12 is forward biased. These conditions create a low impedance circuit path through CR1, FL1, and CR9 to the input of U9, the output amplifier.

Diodes CR3, CR5, and CR1 are reverse biased and thus have a high resistance while CR4, CR6, and CR2 are forward biased and have an extremely low resistance. This prevents any of the 21.4 MHz IF signal (from T1) from reaching FL2, FL3, FL4. Overall isolation exceeds 70 dB.

If the BW code from A1A2 is equal to 10, then U6 would cause CR5 and CR11 to be forward biased, the remaining diodes to be reverse biased, and a signal path to be created through FL3. If the BW code is equal to 01, diodes CR3 and CR10 will be forward biased, creating a signal path through FL2. If the BW code is equal to 11, diodes CR1 and CR9 will be forward biased, creating the signal path through FL1. The selected bandpass filter output from CR9, CR10, CR11, or CR12 (as selected by U6) drives pin 11 of U9, the input of the output amplifier.

3.3.1.1.5 Output Amplifier U9

The output amplifier, U9, is a broadband, high-gain I.C. amplifier. The actual gain of U9 is controlled by a dc current applied to pins 2 and 3. This dc current is derived from the gain adjust voltage from A1A5. The amplified 21.4 MHz IF signal from U9, pin 7, is sent to A1A2. This amplifier provides proper gain-bandwidth compensation.

3.3.1.2 AM/SSB/CW Demodulator A1A2

Refer to Figure 3-4, the AM/SSB/CW Demodulator (A1A2) Block Diagram and Figure 6-2, the AM/SSB/CW Demodulator Schematic Diagram as aids in understanding the following description.

The AM/SSB/CW Demodulator consists of the following components: an input IF amplifier, a log signal strength detector, a wideband/narrowband filter, an AM detector, a BFO, a product detector, an audio switch, a peak detector, a AGC switch, a gain control amplifier, a gain control distribution amplifier, and an AGC threshold timer. The AM/SSB/CW Demodulator facilitates the following actions: amplification of 21.4 MHz IF signals, the AM and CW demodulation of IF signals, and the generation of AGC control voltages to control the overall gain of the demodulator under varying signal conditions.

3.3.1.2.1 Input IF Amplifier Q1, AT1, U2

The 21.4 MHz IF signal input from A1A1 is coupled through transformer T2 to match the input impedance of IF amplifier Q1, a high-gain, dual-gate FET amplifier. The gain of Q1 is varied over a 30 dB range by the dc voltage on gate number 2, pin 2. This dc voltage is derived from the AGC control section and will be discussed in a later paragraph. The amplified 21.4 MHz IF signal at Q1, pin 1, is coupled through tuned matching network C8, C9, C10 and L4 and drives a broadband amplifier, U2.

AT1 is an adjustable attenuator inserted in the signal path between Q1 and U2. It maintains a constant 50 ohms impedance as its attenuation is varied and is used to adjust the overall gain of the demodulator during IF gain alignment. The amplified 21.4 MHz IF signal output of U2, pin 2, drives the input of the wideband/narrowband filter.

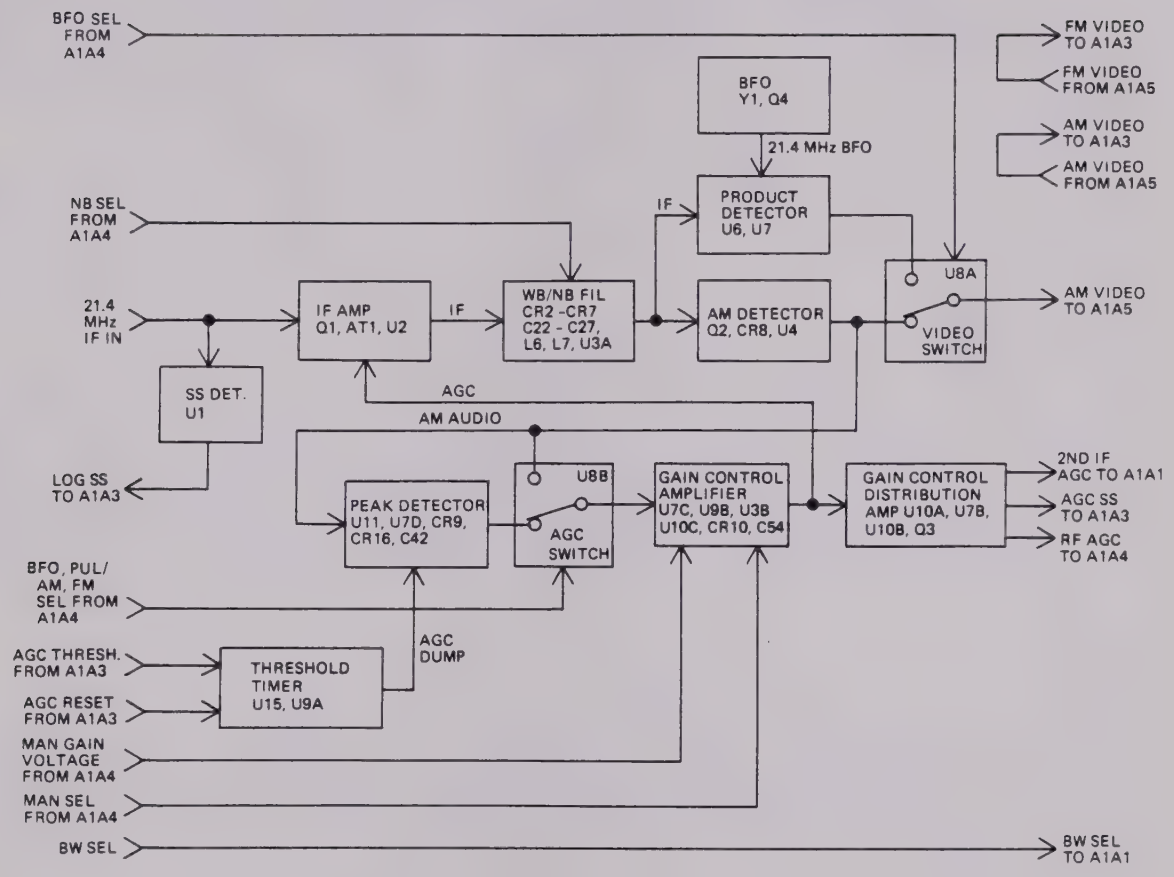


Figure 3-4 AM/SSB/CW Demodulator (A1A2) Block Diagram

3.3.1.2.2 Log S.S. Detector U1

The logarithmic signal strength detector, U1, is an I.C. whose input at pin 15 is driven from the 21.4 MHz IF signal coming from A1A1. The output of U1, pin 13, is a dc voltage whose level varies from 0 to +2 Vdc and is proportional to the logarithm of the actual IF signal level. The output of U1, pin 13, goes to A1A3 as the LOG SS signal.

3.3.1.2.3 Wideband/Narrowband Filter

The wideband/narrowband filter consists of two circuit paths. One is a broadband low-loss circuit and the other is a narrowband double-tuned IF filter circuit. The actual circuit path is selected by the narrowband select signal from A1A4. The narrowband circuit is selected for all bandwidths less than or equal to 200 kHz. The wideband circuit path consists of diodes CR2 and CR4. The narrowband consists of diodes CR3, CR5-CR7, and the double-tuned circuit comprised of C23-C25, C27 and C28, and L6 and L7.

When the narrowband select signal is low, U3, pin 3, is equal to -15Vdc and U3, pin 4, is equal to 0 V. This forward biases diodes CR2, CR4, CR5, CR7, and reverse biases CR3 and CR6. In turn, a low impedance circuit path is provided from U2, pin 2, through CR2, R17, and CR4, and to the input of Q2. The narrowband circuit path is cut off because of diodes CR3 and CR6 being reverse biased and having extremely high resistance.

When the narrowband select signal from A1A4 is high, the U3, pin 3 output is equal to 0 V and the U3, pin 4 output is equal to -15 Vdc. This forward biases CR3 and CR6 and reverse biases CR2, CR4, CR5 and CR7. Therefore a low impedance circuit path exists from U2, pin 2, through CR3, through the narrowband tuned filter and through CR6 to the input of Q2. The wideband circuit path through CR2 and CR4 is cut off because CR2 and CR4 are reverse biased and therefore have high resistance.

3.3.1.2.4 AM Detector Q2, CR8, U4

The 21.4 MHz IF signal from the wideband/narrowband filter is amplified by Q2, and IF buffer amplifier. The output of Q2's collector is coupled through transformer, T1, a tuned circuit centered at 21.4 MHz. The signal is demodulated by CR8, the AM detector. The detected AM signals are filtered and amplified by video buffer amplifier, U4, which is operating at unity gain.

3.3.1.2.5 Beat Frequency Oscillator (BFO) Y1, Q4

The Beat Frequency Oscillator (BFO) is a crystal-controlled oscillator (Q4). The BFO is not used in the IFD121. Y1 is a crystal operating at 21.4 MHz. Q4 is forced to oscillate at 21.4 MHz by Y1 and the resulting 21.4 MHz signal is taken from the collector of Q4 and applied to the input of the product detector. Q4 is energized through switch U9C from the BFO select signal from A1A4. When the BFO select signal is low, U9 output at pin 10 is 0 and Q4 is deenergized. When the BFO select signal is high, the output of U9, pin 10 is +15V. This condition energizes Q4 and causes the BFO signal to be generated and applied to the product detector. The BFO select signal from A1A4 will therefore be high in both BFO and SSB modes and low in FM, CW, AM, and pulse modes.

3.3.1.2.6 Product Detector U6, U7

The product detector, U6, is an I.C. mixer (not used in the IFD121). The 21.4 MHz IF signal from the wideband/narrowband filter is applied to one of the inputs of U6 at pin 4. The BFO signal from Q4 is applied to the other input of U6 at pin 10. U6 mixes the BFO signal with the 21.4 MHz IF signal.

The resultant output signal at U6, pin 12, is an audio signal representing the difference between the two input frequencies. The audio signal is applied to pin 3 of U7, an audio buffer amplifier. The video output at U7, pin 1, goes to the video switch, U8.

3.3.1.2.7 Video Switch U8

The video switch has 2 inputs, pins 2 and 5. Pin 5 is the AM video input from the AM detector whose output is U4, pin 6. U8, pin 2, is the CW/SSB audio input from the audio buffer amplifier, U7, pin 1. The U8 switch is controlled by the CW select signal A1A4. When the CW select signal is high, U8, pin 2, is connected directly to U8, pin 4. The AM video output signal travels from the AM detector through U4, pin 6, to the AM video output. When the CW select signal is high, pin 5 is connected to pin 3 and the AM/CW/SSB video output travels from the product detector through U7, pin 1, to the AM video output.

3.3.1.2.8 AGC Pulse Stretcher U11, U7

The input for the pulse stretching circuit is taken from the AM Video Amplifier, U4. U11, and U7 form a positive peak detector used for pulse, CW, and SSB signals. Capacitor C42 is supplied charging current by U11 through CR16, and holds the peak as CR16 becomes reversed biased when video signal level drops. U7 acts as a high impedance input buffer amplifier and provides loop feedback. The output of U7 is a DC voltage proportional to the peak amplitude of the video signal.

The AGC switch, U8B, is controlled by the CW/Pulse/AM/FM select signal which comes from A1A4. In the AM or FM mode, this signal is high and U8, pin 10, is connected to U8, pin 11. This arrangement connects the video signal from U4, pin 6, to the inverting input of the gain control amplifier U7C. In the CW or Pulse mode, this control line is low and pin 13 is connected to pin 12 of U8. This latter arrangement connects the video signal from U4, pin 6, through the pulse stretcher and then to the input of the gain control amplifier, U7. The use of the pulse stretcher is necessary in the CW and Pulse modes because the signals have a very low duty cycle (signals are present only briefly and then absent for a long period of time). The normal AGC control amplifier will not be able to adequately process the signals in the CW or the pulse mode. The pulse stretcher captures the short pulse width signals in the CW and PULSE modes and holds the IF gain constant.

3.3.1.2.9 Gain Control Amplifier U7, U9, U3, U10

The gain control voltage from either U4, pin 6, or the pulse stretcher through U7, pin 14, is applied to the input of the Gain Control Amplifier and drives U7, pin 9. U7 is a high-gain, dc coupled low pass filter and has a biased threshold point. The output at U7, pin 8, will start moving negative (below 0 Vdc) if the input from the AGC switch U8 exceeds 0.5 Vdc.

The output of U7 travels through the AGC/Manual select switch, U3B. This switch is controlled from the MAN SEL line coming from A1A4. If AGC has been selected as a function, the MAN SEL line is low and the output from U7, pin 8, goes through U8, pin 13, U8, pin 12, and directly to U10C, pin 9. If manual mode has been selected, the MAN SEL line will be high and pins 12 and 13 will open and disconnect the output from U7. U8 pins 10 and 11, are connected, joining the amplifier U10C, pin 9, to the manual gain voltage which comes from A1A4. This manual gain voltage replaces the automatic gain voltage from U7, pin 8, and permits the operator to manually adjust the gain of the demodulator. The voltage from A1A4 is approximately 0 to -10 Vdc.

U10C is a unity gain buffer amplifier. Its output drives the gain control amplifier U10A and the gain controlled amplifier, Q1, pin 2, through U10D. The output of U10D is clamped at -3.7 V by Q5. In normal operation, U10C, U10D and Q5 cause a voltage variation of 0 to -3.7 across CR1. This yields a 30 dB gain reduction through IF amplifier Q1.

3.3.1.2.10 Gain Control Distribution Amplifier

The output from U10C, pin 8 (gain control amplifier,) drives the input of the gain control distribution amplifier, generating three seperate gain control voltage outputs. The signal from U10C, pin 8, drives buffer amplifier-shaping network U10A and U7B. The output of U10A, pin 1, goes to U7, pin 5. A diode network (CR12 and CR15) and biasing resistors (R64, R65, R61, R62) define two linearizing break points which partially linearize the operating characteristics of attenuator A1A1G1. The voltage at U7, pin 5 is automatically shaped by the linearizing network. The output from U7, pin 7, is the second IF AGC voltage and is sent to A1A1 to control the gain of A1A1G1.

The output at U10A, pin 8, also drives the input of U10B, pin 5. The output from U10B, pin 7, takes two seperate paths. The first path travels through CR13 to become the AGC signal strength voltage which is sent to A1A3. U10B is threshold biased by R89 and R88. The output at U10B pin 7 does not begin to rise until the dynamic range limit of Log SS detector U1 has been exceeded. The second output from U10B through R86 is the RF AGC voltage which is not used in the IFD121.

3.3.1.2.11 AGC Threshold Timer U15, U9

The AGC threshold timer consists of U15, a dual monostable multivibrator, and an analog switch, U9A. U9A and U15 provide a means of discharging C42 (the peak value of CW or Pulse signals.) The pulse stretcher charges to the highest amplitude of the signal, but when this level drops to a no-signal level, the AGC threshold timer discharges or resets the peak detector after a 250 msec delay.

The TRIG and RESET inputs to U15 come from A1A3 which monitors the signal strength voltage. The signal strength voltage is the sum of LOG SS and AGC SS voltages. When the signal strength is above a threshold point, the RESET input to U15 will be low, disabling U15. In CW or Pulse modes, if the signal strength voltage on A1A3 drops below the threshold, the RESET input to U15 goes high, and a short TRIG pulse is applied to U15 pin 6. 250 msec later, a short +15 Vdc pulse is output from U15, pin 9. This action momentarily closes switch U9A, pins 3 and 2, and discharges C42 to 0 V. Several milliseconds later the output of U15, pin 9, is recovered, switch U9A opens, and C42 charges to the new lower voltage level of the signal.

3.3.1.3 Video/Audio A1A3

Refer to Figure 3-5, the Video/Audio (A1A3) Block Diagram and Figure 6-3, the Video/Audio Schematic Diagram as aids in understanding the following description.

The video/audio module consists of the following components: an AM video amplifier, an FM video amplifier, an audio amplifier, a LOG SS peak detector, an SS combiner/amplifier, and an SS comparator. The video/audio provides for the output amplification of AM and FM video signals, for the selection of rear panel audio signals, and for the development of the AGC signal strength voltage.

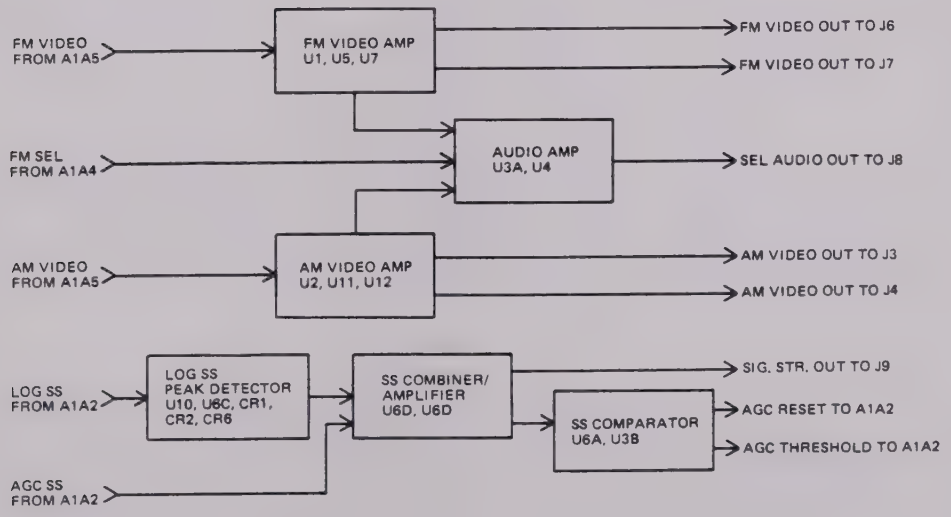

FM VIDEO FROM A1A5
FM VIDEO AMP U1, U5, U7
FM VIDEO OUT TO J6
FM VIDEO OUT TO J7
FM SEL FROM A1A4
AUDIO AMP U3A, U4
SEL AUDIO OUT TO J8
AM VIDEO FROM A1A5
AM VIDEO AMP U2, U11, U12
AM VIDEO OUT TO J3
AM VIDEO OUT TO J4
LOG SS FROM A1A2
LOG SS PEAK DETECTOR U10, U6C, CR1, CR2, CR6
SS COMBINER/ AMPLIFIER U6D, U6D
SS COMPARATOR U6A, U3B
SIG. STR. OUT TO J9
AGC RESET TO A1A2
AGC THRESHOLD TO A1A2
AGC SS FROM A1A2

Figure 3-5. Video/Audio (A1A3) Block Diagram

3.3.1.3.1 AM Video Amplifier U2, U11, U12

AM video signals from A1A5 are applied to the AM video amplifier at U2, pin 3. U2 is an adjustable gain buffer amplifier which provides an overall voltage gain of approximately 4. The output at U2, pin 6, drives the two unity buffer output amplifiers U11 and U12. These amplifiers generate high output drive current; both develop the two AM video outputs which are routed to the rear panel connectors, J3 and J4. The output from U2, pin 6, is also sent to the input of the audio amplifier through analog switch U3A.

3.3.1.3.2 FM Video Amplifier U1, U5,U7

FM video signals from A1A5 are applied to the FM video amplifier at U1, pin 2. U1 is a buffer amplifier with an overall voltage gain of approximately 5. The output at U1, pin 6, drives the two output buffer amplifiers, U5 and U7. These are broadband unity gain buffer amplifiers which provide high output drive current and develop the two FM video output signals which are routed to two rear panel connectors, J6 and J7. The output of U1, pin 6, also drives the input to the audio amplifier through analog switch U3A.

3.3.1.3.3 Audio Amplifier U3, U4

The audio amplifier selects one of two inputs: the AM video input from U2, pin 6, or the FM video input from U1, pin 6. The selection is controlled from A1A4. The FM select line controls audio switch U3. When the FM select line is low, the output from U2, pin 6, is coupled through U3, pin 2, to U3, pin 3, and applied to U4, pin 2. When FM select is high, the output from U1, pin 6, is coupled through U3, pin 5, to U3, pin 4, and to U4, pin 2. U4 is a buffer amplifier with a voltage gain of approximately +3. The AM or FM signal selected by U3 is amplified by U4. The output from U4, pin 6, is the selected audio output which is routed to the rear panel connector, J8.

3.3.1.3.4 LOG SS Peak Detector U10, U6

The LOG SS signal from A1A2 drives a peak detector comprised of U10, U6, CR1, and CR2. C26 is charged by U10 to a positive voltage which is equal to the peak value of the voltage applied to U10, pin 3. This reduces the level of the audio signal on the LOG SS input. The output at U6, pin 8, drives one of the inputs to the SS summing amplifier.

3.3.1.3.5 SS Summing Amplifier U6

The SS combiner amplifier has two inputs. One input, from U6C, pin 8, is the peak value of the LOG SS signal from A1A2. The other input is the AGC SS voltage from the AGC circuitry on A1A2. These two voltages are summed at the input of U6D, pin 13. U6D operates at a voltage gain of approximately unity for the AGC input and at +3 for the LOG SS input. The output of U6D, pin 14, represents the sum of the AGC and LOG SS inputs. This signal is inverted by unity gain inverter, U6B. The output at U6B, pin 7, then drives the input of the SS Comparator and is also routed to rear panel connector J9 for the signal strength output of 0 to 10 Vdc.

3.3.1.3.6 SS Comparator U6, U3

I.C. U6A is a voltage comparator. The voltage at pin 2 is biased at approximately 1.5 Vdc. The other input at U6, pin 3, monitors the strength of the voltage from the signal strength summing amplifier. If the output at U6B, pin 7, is greater than 1.5 Vdc, the output at U6A, pin 1, is high. This drives the the input to switch U3, pin 9, and it holds pin 11 to ground while pins 12 and 13 are open. These conditions presuppose that the AGC threshold output from U3 is grounded. If the voltage at U6, pin 7, drops below +1.5 Vdc because of a drop in input signal level, then the signal is below the AGC threshold defined by U6A. This brings the output low at U6A, pin 1, which causes U3B to switch, closing pins 12 and 13. Concurrently, pins 10 and 11 open, sending high reset signal to A1A2 which energizes the timer on A1A2. A TRIGGER pulse is sent through C33 to A1A2 which triggers the timer and resets the AGC peak detector on A1A2 after 250 milliseconds.

3.3.1.4 FM Demodulator Motherboard A1A5

Refer To Figure 3-6, the FM Demodulator (A1A5) Block Diagram, and Figure 6-5, the FM Demodulator Schematic Diagram as aids in understanding the following description.

The FM demodulator motherboard consists of four FM demodulator modules, an AM video multiplexer, an FM video multiplexer, and a demod select/gain adjust multiplexer. The FM demodulators provide for FM demodulation of the 21.4 MHz IF signal and routing of the AM video signals through the AM video low pass filters.

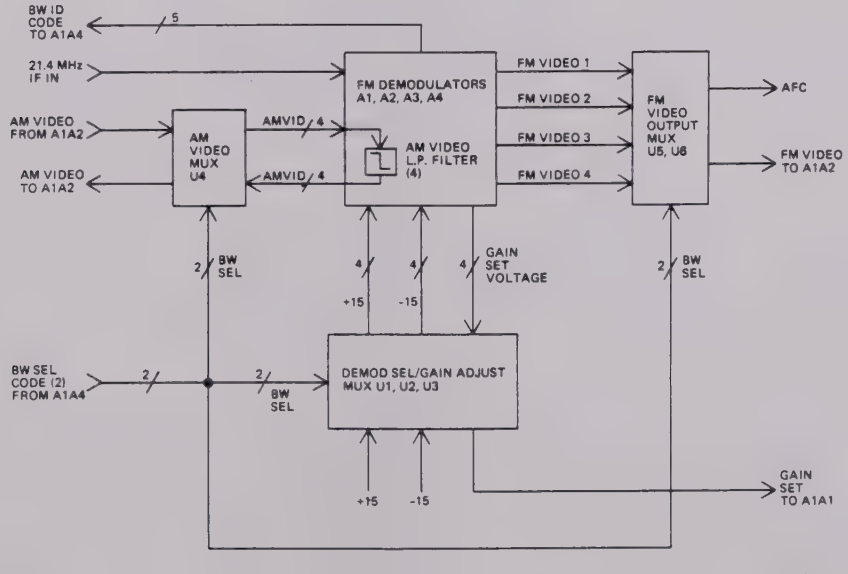


Figure 3-6. FM Demodulator (A1A5) Block Diagram

3.3.1.4.1 FM Demodulator, A1, A2, A3, A4

FM demodulator modules A1 through A4 have four different bandwidths, each corresponding to the bandwidth of a matching bandpass filter in A1A1. The four bandwidths of the FM demodulators are 150 kHz, 500 kHz, 1 MHz, and 4MHz. The 21.4 MHz IF input signal from A1A2 drives the common input to all four of the demodulator units on P3-1. These modules are field-changeable to accomodate different IF bandwidths.

When slected, each demodulator module when selected is energized by +15 Vdc on P1-11 and -15 Vdc on P2-1. This energizing voltage is provided by the Demod Select/Gain Adjust Multiplexer which decodes the BW Select Word from A1A4. Each demodulator module is assigned a 5-bit bandwidth ID code. During power up, the software initializing routine successively energizes the BW ID network on each demodulator module. The BW ID codes are then read back into the Digital Interface, A1A5, which keeps a record of the actual bandwidth of each module as installed.

There are two types of FM demodulator modules used in the IFD121 IF Demodulator. A narrowband version is used for the 150 kHz bandwidth module and a wideband version is used for the 500 kHz, 1 MHz, and 4 MHz bandwidth modules.

Figure 3-7 is a block diagram of the narrowband FM demodulator module. Figure 6-6, FM Demodulator (30-200 kHz) Schematic Diagram, may be referred to for greater detail. The 21.4 MHz IF input signal from A1A2 is amplified and limited by wideband amp/limiter U1. The U1 output is coupled to differential peak detector L1,C7,C8 and C6. Below 21.4 MHz, C11 series resonates with the tank circuit, developing maximum IF voltage across C11. The IF voltage is detected by CR2 which sends a negative voltage to the noninverting input of U2A. Above 21.4 MHz, C11 bypasses the tank circuit, developing maximum IF voltage across L1. The IF voltage is detected by CR1 which sends a negative voltage to the noninverting input of U2B. The output at U2A-1 is a composite of the two negative voltages, representing the typical FM demodulator "S-curve". The low level FM video from U2A B is amplified by the video buffer, U2C, and lowpass filter, L4-C20, to give a high level FM video output to the video multiplexer via P1-2. The AM video signal from A1A2 is routed through the low pass filter. This filter establishes an effective AM Video bandwidth of 100 kHz. The filter output is routed back to A1A2 for further processing. The bandwidth ID network consists of R3 and CR5-CR7 (CR3 and CR4 are not present.) This gives a bandwidth ID of 00111 for the 150 kHz module which is read by the digital interface during power up, as explained previously.

Figure 3-8 is a block diagram of the wideband FM demodulator module. Figure 6-7, FM Demodulator (300 kHz - 4 MHz) Schematic Diagram, may be referred to for greater detail. The 21.4 MHz IF input signal from A1A2 is amplified and limited by wideband amp/limiter U1. The IF output from U1 is applied to the Discriminator. The Discriminator is center-tuned to 21.4 MHz and establishes the necessary phase shifts to convert wideband FM to amplitude variations. These variations are detected by CR1 and CR2 and amplified by video buffer U2. They are lowpass-filtered at 1/2 the IF bandwidth by L2 and C14 to give a high level FM video output to

the video multiplexer via P1-2. The AM video signal from A1A2 is lowpass-filtered by L3 and C5 to approximately 0.7 times the selected IF bandwidth. The filter output is routed back through A1A2 to A1A3 for video and audio outputs. The bandwidth ID network consists of R11, R12 and combinations of diodes CR3 through CR7. The following chart shows the combinations of diodes and ID codes for each of the wideband modules.

BW	DIODES USED	BW ID CODE
500 kHz	CR3, CR5	10100
1 MHz	CR3, CR5, CR7	10101
4 MHz	CR3, CR5, CR6, CR7	10111

The video outputs from the four FM demodulators are routed through the video multiplexer and are explained in paragraph 3.3.1.4.3. The AM video outputs from the four FM demodulators are routed through the AM video multiplexer and are explained in paragraph 3.3.1.4.2.

Each FM demodulator module also provides a fixed gain set current output to A1A1U9. The current is derived from the +15 Vdc supply through a dropping resistor (R16-narrowband, R13-wideband.) The gain set current appears at P1-3 of the active FM demodulator module and is routed through the Demod Select/Gain Adjust Multiplexer. It is then sent through A5P5 to A1P1 where it provides gain bandwidth compensation by adjusting the gain of A1A1U9 for the installed IF bandwidth.

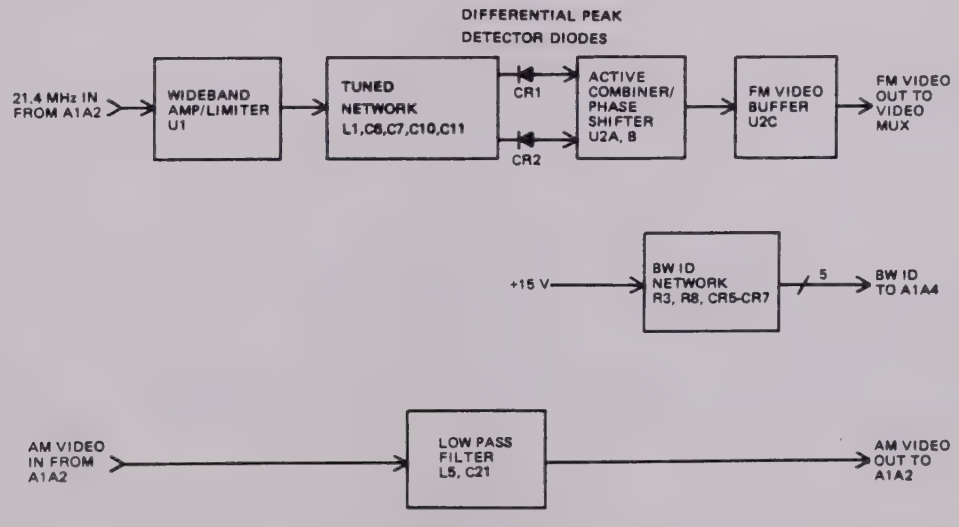


Figure 3-7. FM Demodulator (10-200 kHz BW)

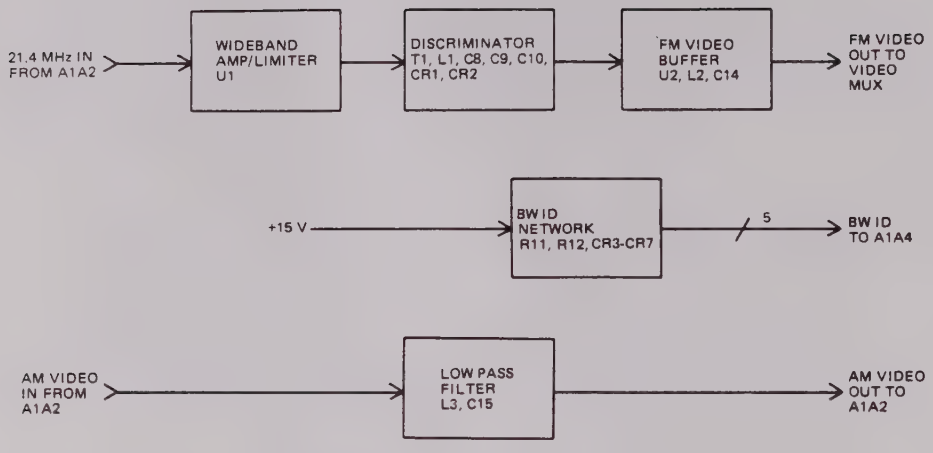

21.4 MHz IN FROM A1A2
WIDEBAND AMP/LIMITER U1
DISCRIMINATOR T1, L1, C8, C9, C10, CR1, CR2
FM VIDEO BUFFER U2, L2, C14
FM VIDEO OUT TO VIDEO MUX
+15 V
BW ID NETWORK R11, R12, CR3-CR7
5
BW ID TO A1A4
AM VIDEO IN FROM A1A2
LOW PASS FILTER L3, C15
AM VIDEO OUT TO A1A2

Figure 3-8. FM Demodulator (300 kHz - 4MHz BW) Block Diagram

3.3.1.4.2 AM Video Multiplexer U4

The AM video multiplexer, U4, is a two-section addressable analog multiplexer. The address inputs enter on pins 9 and 10 and are driven by the bandwidth code from A1A4. This two-bit code enters U4, which has two separate sections. Each section has one analog input and four analog outputs. The two address inputs therefore select one of the four outputs. The multiplexer routes the AM video input to the selected FM demodulator for AM video filtering and then routes the output of the lowpass filter to AM video output P2.

If a code of 00 exists at the inputs, output number one is selected (U4, pins 1 and 12.) If a code of 01 is received at the input pins, output number two is selected (U4, pin 5 and 14.) If a 10 is received, output number three is selected (U4, pin 2 and 15.) If an 11 is received at the input pins, output number four is selected (U4, pin 4 and 7.) U4, pin 3, is the AM video input from A1A2; the signal will go through that half of U4 and the AM video signal will appear at pins 1, 5, 2, or 4 as selected by pins 9 and 10 (address inputs.)

Assuming an address code of 00 is received at input pins 9 and 10, the AM video through pin 3 will appear at U14, pin 1, and will go to P1, pin 9, on demodulator module A1. Internally it will be lowpass-filtered in A1 and will appear on P1, pin 10, to U4, pin 12. Pin 12 is connected to pin 13 (since the input was 00) and the output will be sent through A1A2 to A1A3 video/audio as the filtered AM video signal.

3.3.1.4.3 FM Video Output Multiplexer U5, U6

The FM video output multiplexer is composed of analog switch U5 and buffer amplifier U6. U5 is an analog multiplexer with two address inputs at pins 10 and 9, driven from the bandwidth select code from A1A4. U5 has four inputs (pins 1, 5, 2, 4) and a single output at pin 3. A code of 00 on pins 10 and 9, will connect pin 1 to pin 3. A code of 01 will connect pin 2 to pin 3, a code of 10 will connect pin 5 to pin 3, and a code of 11 will connect pin 4 to pin 3.

U5 receives as its input the four video signals from the four FM demodulator units. Only one will be active at a time. An input of 00 to pins 10 and 9 of U5 means that the FM video output of module A1 (P1, pin 2,) goes to U5, pin 1, through U5, pin 3. The signal is then routed through A5P1 and and A1A2 to A1A3 video/audio module. The signal also goes to buffer amplifier, U6, a high-gain dc-coupled buffer amplifier (operating as a low pass filter.) The output of U6, pin 6, is used as an AFC voltage to generate an error correction voltage to the host unit (external) driving the demodulator.

3.3.1.4.4 Demod Select/Gain Adjust Multiplexer U1, U2, U3

The demod select/gain adjustment Multiplexer performs two functions. The first function is to select which one of the four demodulators is to be active. The second function is to route the selected demodulator's gain adjust output current through the gain adjust line to A1A1.

U2 is a dual analog multiplexer which is similiar in operation to U4. U2 has two separate sections with each having four inputs and one output. U2 is addressed at pins 10 and 9 from the bandwidth select code coming from A1A4.

One-half of U2 sends +/-15 Vdc to the correct demodulator to be energized; the other half is used to process the gain adjust current for the desired demodulator. Example: 00 is input to pins 10 and 9. U2, pin 12, will be connected to U2, pin 13, effectively placing +15 Vdc on the control pin U1, pin 6. These conditions cause U1, pin 2 to be connected to U1, pin 3, and U1, pin 5, to be connected to U1, pin 4. This sends +15 Vdc to demodulator unit A1, P1, pin 11, and also a -15 Vdc to demodulator unit A1, P2, pin 1. Therefore the 00 sent to U2 energizes FM demodulator A1. A code of 00 sent to U2 also connects pin 1 to pin 3 which connects the gain adjust current from demodulator unit A1 to the P5, gain set output to A1A1U9. The same principles apply to codes 01, 10, and 11 being applied to input pins 9 and 10. Pin 3 will be connected to pin 1, 5, 2, or 4 of U2 which are the gain adjustment current outputs of FM demodulators A1, A2, A3, and A4.

3.3.1.5 Wideband IF Amplifier A2A1

Refer to Figure 6-8, IF Demodulator Main Chassis Schematic Diagram, as an aid in understanding the following description.

The wideband 21.4 MHz IF output signal from A1A1 drives the input of the wideband IF amplifier. The IF signal enters on terminal E1. It then couples through C2 and resistor network R2 and R3 to drive the input to RF amplifier U1 at pin 1. U1 is a broadband hybrid RF amplifier with an overall gain of approximately 14 dB. The amplified wideband IF output at U1, pin 2, is coupled through C4 to power splitter U2.

U2 has two outputs, pin 2 and 4. Each output is approximately 3.5 dB lower in signal level than the input of U2, pin 1. Each output from U2 is made available as a wideband IF output (21.4 MHz). The two outputs are A1J1 and A1J2. Operating power for I.C. U1 is derived from circuit card A1A1 over the signal carrying line; the signal is decoupled through R1, C1, L1, and R4 to provide DC power to U1.

3.3.2 DIGITAL CONTROL SECTION

Refer to Figure 3-9, Digital Control Section Block Diagram, as an aid in understanding the following description.

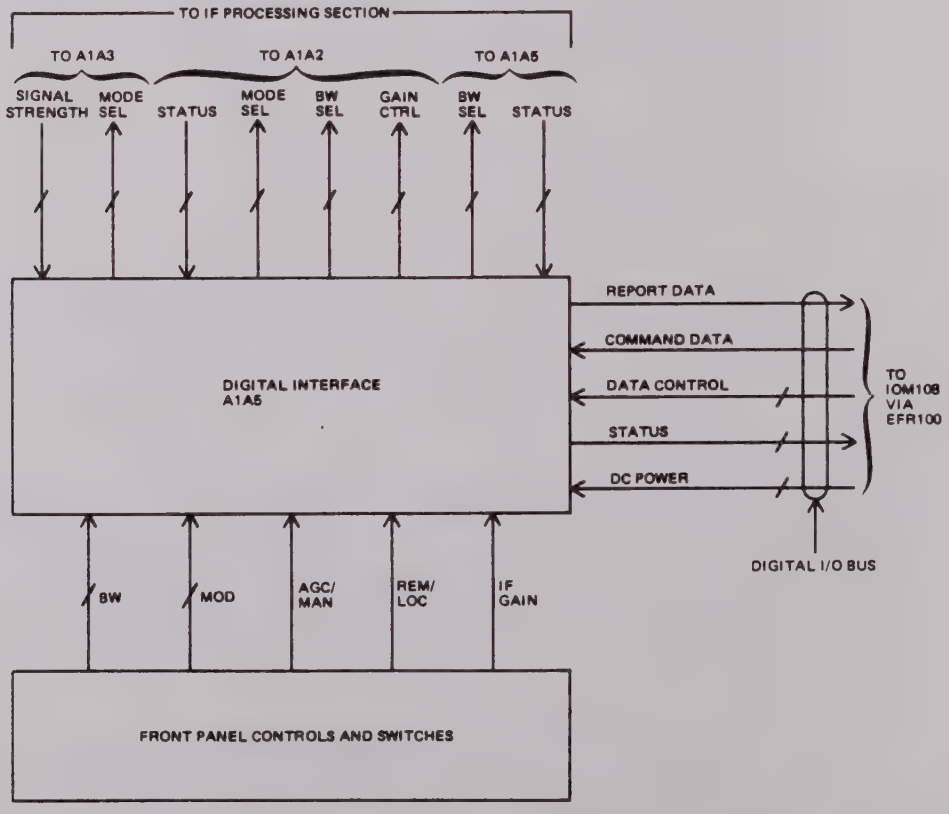


Figure 3-9. Digital Control Section Block Diagram

As shown in Figure 3-9, the Digital Control Section consists of the following major assemblies:

a. Front Panel Controls and Switches

b. Digital Interface, A1A4

c. Digital I/O Bus

The central element of the Digital Control Section is the Digital Interface assembly, A1A5, which coordinates all control and status data flow within the demodulator. The front panel controls and switches provide the operator input interface to the demodulator. The Digital I/O Bus provides for remote operation of the demodulator via an external controller such as the IOM108.

3.3.2.1 Front Panel Controls and Switches

Refer to Figure 6-8, IF Demodulator Main Chassis Schematic Diagram, as an aid in understanding the following description. The front panel inputs are connected directly to the digital interface via A1A4P1. The IF BW and DETECTION MODE switches are configured to provide a logic low to the digital interface for the selected mode or BW. Unselected modes and BW's are pulled to logic high by the digital interface. The gain control switch is configured to provide a logic high when MAN is selected and a logic low when AGC is selected. The local/remote switch provides a low when remote is selected and is pulled high when in local. The IF GAIN control potentiometer is driven from a -15 Vdc source on the digital interface. Varying the IF GAIN from minimum to maximum provides a variable 0 to -10 Vdc IF GAIN VOLTS input to the digital interface.

3.3.2.2 Digital Interface A1A4

Refer to Figure 3-10, Digital Interface (A1A4) Block Diagram, and Figure 6-4, Digital Interface Schematic Diagram, as aids in understanding the following components:

The digital interface is a single printed circuit card consisting of a CPU, address latch, EPROM, address decoder, serial I/O, interrupt circuit, D to A converter, BW mode latch, BW ID, buffer, and a polled I/O Analog switch.

The digital interface receives control inputs either from the front panel in local mode or from the WJ-9040 I/O Bus in the remote mode of operation. It then generates the control signals to program the IF Processing Section of the demodulator.

3.3.2.2.1 CPU U1

The CPU, U1, is an 8031 CMOS microcontroller (CPU) containing 128 bytes of internal RAM. It requires an external ROM for proper operation. It operates at a 10 MHz rate, determined by crystal Y1, and has a 1.2 microsecond instruction cycle. The CPU is a self-contained device with the exception of an external EPROM which contains the system operating software.

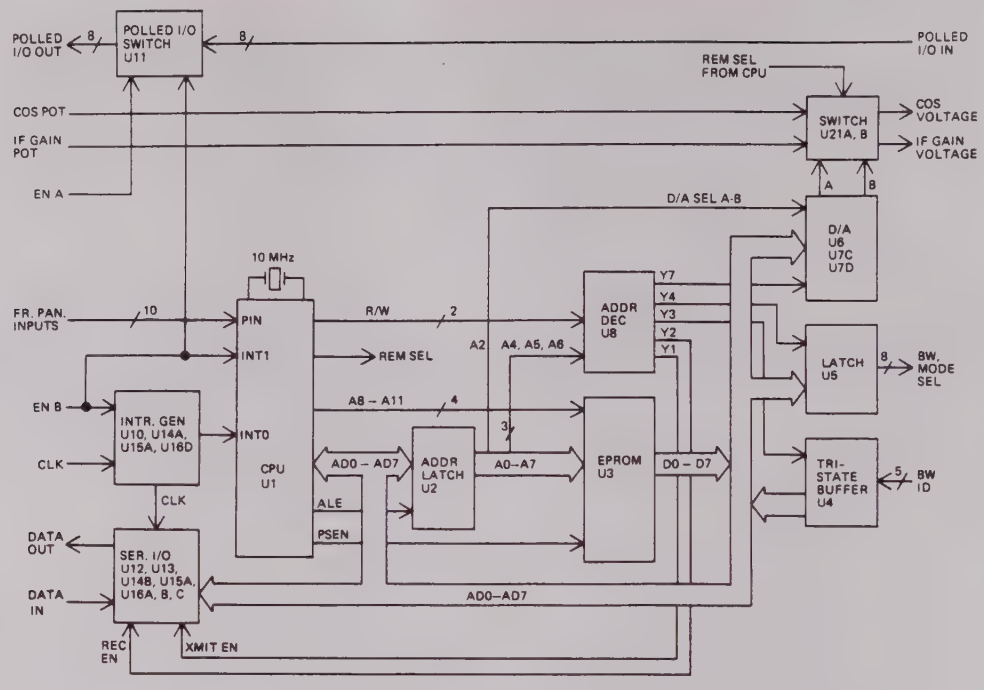


Figure 3-10. Digital Interface (A1A4) Block Diagram

The RC circuit connected to the CPU Reset Input, pin 9, pulses high when power is applied to the digital interface, This resets all the internal hardware registers and starts the CPU at addresses 00.

The program then performs an initialization routine which both sends data to and initializes the CPU. The CPU has four 8-bit I/O ports, P0 through P3. The initialization routine determines the functions of each of these ports.

A total of 11 bits of data (P1.0 through P1.7 and P3.0, P3.4, and P3.5) are configured for the front panel I/O port. This port receives the control signals from the front panel control switches.

The INT 0 (P3.2) and INT 1 (P3.3) signals will be used when using the WJ-9040 I/O Bus in remote control.

The P0 port (a bidirectional address/data bus) allows the CPU to communicate with the circuitry on the card or off the card using the WJ-9040 I/O bus. The P0 port contains 8 address lines, AD0 through AD7, but 12 address lines are necessary for addressing within the demodulator. The remaining 4 address lines (A8 through A11) defined as P2 complete the necessary address lines for the CPU. A12, P2.4 thru A15, and P2.7 are not used.

The REM/SEL output, P3.1, is used (local when high, remote when low) to control COS and IF gain analog switches.

The RD (P3.7), and WR (P3.6), lines are used only for external data transfers within the demodulator or through the WJ-9040 I/O Bus to the other units.

The ALE (Address Latch Enable) output is toggled from a high to a low to clock valid address data out on the AD0 - AD7 lines. Address latch U2 holds the valid address for one complete cycle.

The PSEN line is used during an opcode fetch from the EPROM (U3.) When a transfer is required, the PSEN will momentarily go low and data will be transferred from the EPROM to the CPU.

The address data bus is an 8-bit bus connecting several devices on the card. The outputs from U1, U4, and U3 are tri-state outputs (when these devices are not active, they are disconnected from the address bus.) Only one of these devices may be active at a time.

3.3.2.2.2 Address Latch U2

The address latch is an 8-bit latch which will hold an address coming from U1 while a specific operation is being performed. The AD0-AD7 outputs are not valid for an entire bus cycle, so that the address latch must hold this address by activating the ALE signal to a high then a low level. This action will transfer the D inputs to the Q outputs which remain until a new address is sent to U2. The outputs of U2 drive the address inputs to U8 (A,B,C) and U3 (A0 to A7) and the DAC A/DAC B input to U6.

3.3.2.2.3 EPROM U3

The EPROM contains 4K x 8 memory. It has an input address range of 0000 to FFFF. The EPROM also has an 8-bit data bus output Q0 to Q7. The eight lower address bits are received directly from U2 and the upper four bits are received from U1.

In a typical operation an address will be presented to U3 (AD0 through AD7 plus A8 through A11) by the CPU. With a valid address present at U3, the CPU will pulse the PSEN line to a low and the addressed memory data is available at the outputs of Q0 to Q7 to be placed on the address data bus. The Q0 to Q7 outputs will only be present on the bus while the PSEN line is held low.

3.3.2.2.4 Address Decoder U8

The address decoder is used to define external I/O operations. The address decoder is used to select data transmit or receive through the serial I/O circuit, to activate the BW I.D. buffer, to activate the BW mode select latch, and to activate the D/A converter.

U8 is a 3-bit to 8-bit decoder. It is addressed by three binary bits on inputs A,B, and C. The input value has a range of 000 to 111. With 000 placed on the A,B, and C inputs, the Y0 output would go low. With 001 on the input lines, Y1 would be active and so on. Refer to the following example:

INPUTS A B C	OUTPUT ACTIVATE
0 0 0	Y0
0 0 1	Y1
0 1 0	Y2
0 1 1	Y3
1 0 0	Y4
1 0 1	Y5
1 1 0	Y6
1 1 1	Y7

The G2A enable input is driven by the RD and WR lines from U1 and is used to enable U8.

The A,B, and C, address inputs are driven by bits A4,A5 and A6 from the address outputs of U2. While U2 has 16 address bits, the least significant eight are used for external device addressing.

To utilize U8, U1 will send an address over the AD0 to AD7 lines, latch it through U2, and on to U8. Three outputs on U8 are not being used: Y0, Y5 and Y6. The first valid output on U8 is therefore Y1. Y1 is the transmit enable line to the serial I/O circuitry. To activate Y1, 0000 (Q0-Q3) and 1000 (Q4-Q7) which equals 10 in hexadecimal is sent from U2 to U8. Simply stated, a hexadecimal address of 10 is sent from the CPU, through U2 to U8, activating the Y1 output. The Y2 output (serial I/O receive enable line) is activated when a hex address of 20 is received from U2. The Y3 output to the tri-state buffer is activated when a hexadecimal address of 30 is received from U2. The Y4 output to the BW mode select latch is selected when a hex address of 40 is received. The Y7 output selects the A portion of the D/A converter (U6) when a hex address of 70 is received from U2. With a hex address of 74 (Y7 from U8 and Q2 from U2,) the B portion of the D/A converter will be selected. The Y0 through Y7 outputs are active low signals.

HEX ADDRESS	U8 OUTPUTS
10	Write Data/ Transmit Enable to Serial I/O circuit
20	Receive Enable / Read Data to Serial I/O circuit
30	Enable B/W ID Buffer (U4)
40	Enable Mode BW Latch (U5)
70	Enable D/A Converter Section A
74	Enable D/A Converter Section B

3.3.2.2.5 Interrupt INT0 and INT1:

Data transfers between the demodulator and an external controller are serial synchronous and are made up of three signals: CLK, Enable B, and Data (Input or Output.) The CLK and Enable signals are used to interrupt the CPU so that a data transfer function must be performed.

The eight clocks interrupt circuit consists of AND Gate U14A, counter U10, and an inverter U16D. Data is clocked in or out eight bits at a time. Counter U10's output is inverted and on the following edge of the eight count interrupts the CPU to read or write the data byte. When a data read is performed the U10 counter is reset to 0 and is ready for another byte of data.

The enable B Input INT1 is a high to low edge triggered interrupt. When the Enable B signal goes high to enable the data transfer and then returns low at the end of the data message, the CPU stops what it is currently doing and performs the function according to the message received.

3.3.2.2.6 Serial I/O U12, U13, U14, U15, U16

The serial I/O is a bidirectional parallel-to-serial, serial-to-parallel transmitter/receiver circuit. It consists of U12, a serial-to-parallel converter, and U13, a parallel-to-serial converter. U12 and U13 are driven by a gated CLK U14A. U13 is enabled by the transmit enable line Y1 from U8. U12 is enabled by the receive enable line Y2 from U8.

When the demodulator receives data from the IOM108, enable B will go high and eight clocks are received causing the data to be clocked into the device U12. The input INT0 goes low, interrupting the CPU to read a byte of data from serial to parallel device U12 by the Y2 output of U8. After the last byte of data has been received, the enable B signal INT1 is reset and notifies the CPU to process the data received.

A data transfer from the demodulator to the IOM108 is a similar function. A data byte is loaded into the parallel to serial device U13 by the Y1 output of U8. Enable B goes high and eight clocks are received shifting the serial data out. This interrupts the CPU to load up another byte of data for the IOM108 to read or an Enable B interrupt occurs to finish the cycle.

3.3.2.2.7 D/A Converter U6

The D/A Converter and analog switch U21A and B are used to control IF gain and set COS threshold voltage in the remote mode of operation.

The D/A converter has 8 data bits at its input lines D0 through D7 and a voltage output at VA. If all of the data inputs are low, the output at VA is equal to 0 Vdc. If the data inputs are all high, the output at VA will be 2.5 Vdc. Each one bit increment or change at the input causes the voltage to change by approximately 10 millivolts. The output of VA is amplified and inverted by U7D to produce a voltage range at the output of 0 to -10 Vdc.

The B section of this converter is used for the COS threshold voltage. The COS threshold is not used in this demodulator. The operation would be similar to the gain operation except that the VB amplifier output would range from 0 to +10 Vdc.

When the local mode of operation has been selected at the front panel, the REM select line will go high. This connects the front panel IF gain potentiometer wiper on J5, pin 5, to the demodulator gain circuit at J3, pin 11, through pins 4 to 5 of U21A. This voltage varies from 0 Vdc for minimum gain to -10 Vdc for maximum gain. When remote mode is selected, the output of D/A U6 through amplifier U7D is connected to the demodulator gain circuit through pins 3 to 2 of U21A.

U21B controls COS voltage in an identical manner.

3.3.2.2.8 Bandwidth/Mode Latch U5

U5 is an 8-bit octal latch similar to Address Latch U2. Inputs to U5 consist of the eight bits from the data bus (AD0 through AD7). The Q1 through Q4, Q6, and Q7 outputs of U5 are used to define the mode and bandwidth selection for the IF processing section and exit the digital interface card via J3. The Q0 output is a Read Request bit to let the controller know when a demodulator needs service. It is sent to the polled I/O Switch, U11. The Q5 output exits the card via J2, pin 3, to produce the FM select signal.

In a typical operation, the CPU (U1) examines the front panel inputs on the I/O port of the CPU every 3 milliseconds. If there is a change in the front panel inputs, the CPU puts the BW/mode select data word on the data bus to the D inputs of U5. The new BW/mode data is latched to the Q outputs and connected to the IF Processing Section when the address decoder U8 Y4 output goes from a low to a high.

3.3.2.2.9 Bandwidth I.D. Buffer U4

The bandwidth I.D. is the unique code assigned to each of the four demodulator modules as explained in paragraph 3.3.1.4.1.

During the power-up initialization routine, the CPU examines each of the four FM demodulator modules and reads the BW I.D. present on each card. The BW I.D. is brought in through U4 and placed on the data bus to the CPU memory. This way, the CPU knows which FM demodulator to energize when it receives the request from one of the four bandwidths.

Five inputs (U4 pins 2,4,6 and 11) comprise the BW I.D. information. During the initialization routine, the CPU selects the FM demodulator #1. The BW I.D. code enters U4 which is selected by the Y3 output of U8 (hexadecimal address of 30). The BW I.D. information is then placed on the data bus (AD0 through AD4). The BW I.D. of FM demodulator #1 is then transferred into the memory of the CPU. BW I.D.'s #2, #3 and #4 are similarly processed.

Inputs 13, 15, and 17 to U14 are not used in this configuration. Therefore, outputs AD5 through AD7 are not used.

The BW I.D. code is also used to define a configurator, a 16-bit data word that defines this unit i.e., operating frequency range, bandwidths available, etc. It is used by the systems 9040 controller so that the 9040 controller can identify what this unit is, what it contains, and its purpose in the system, i.e., which demodulator and what its bandwidths are.

3.3.2.2.10 Polled I/O Switch U11

This analog switch is used by the 9040 controller to extract information from the demodulator using the Enable A and Enable B inputs. The Enable B input will transfer the READ REQ, SIG STR, and COS STATUS (J1, pin 20, 18, 25) to the polled I/O bus to the IOM108. The COS STATUS is not used in this unit.

The SIG STR entering from J2, pin 7, would be passed through U11, pin 11, to J1, pin 18, to the IOM108 when energized by the Enable B input. The Read Request output from U5, pin 2, is connected to U11 pin 14. The Read Request signal is active low and when the Enable B signal enables U11. The Read Request is then connected to the bus through U11, pin 15, to the IOM108 to be read.

The SEL AUDIO signal entering from J2, pin 6, will be passed through U7A and U11, pin 3, to the IOM108 via J1, pin 22, when U11 is energized by the Enable A input. The Enable A signal is only active for the demodulator that has been selected by the IOM108.

3.3.2.3 Digital I/O Bus

The digital I/O bus is shown in Figure 3-9. Additionally, Figure 6-4, Digital Interface Schematic Diagram, should be referred to as an aid in understanding the following description. When operated by an external controller (the IOM108 I/O module,) the digital interface connects to the controller using serial to parallel and parallel to serial converters. Actual communication occurs via the WJ-9040 Digital I/O Bus through the EFR100 frame to the IOM108. As shown in Figure 3-9, these lines consist of report data, command data, data control and polled I/O.

The command data line is a serial data line. The external controller uses this line to transfer demodulator parameter data and communication commands to the digital interface. Data on this line is clocked through a serial to parallel converter and then is transferred to the microcontroller via the address/data bus.

The report data line is a serial data line. It is used to send data from the demodulator to the controller through a parallel to serial counter and to report a unique serial data word called the configurator. This word is generated by the demodulator software and defines the hardware type, tuning range, bandwidths available, and options. The configurator is used by the IOM108 to construct a WJ-9040 System master list in its software.

The data control lines are generated by the external controller and are used to coordinate the transfer of command and report data between the digital interface and the external controller. They consist of the Enable B, Enable A and CLK lines.

SECTION IV

MAINTENANCE

4.1 GENERAL

This section contains maintenance procedures for the IFD121 IF Demodulator. Included are preventive maintenance procedures, performance verification tests, troubleshooting and fault isolation procedures, and alignment procedures.

4.2 MODULE ACCESS

The following procedures are to be used to gain internal access to the demodulator modules.

4.2.1 MODULES A1A1, A1A2, AND A1A3

To gain access to A1A1, A1A2, or A1A3 proceed as follows:

1. Disconnect cables from A1J3, A1J5, A1J7 and A1J8 on the top of the demodulator.

2. Remove two screws on the rear of A1. Remove top and bottom screws on the front of A1.

3. Pull A1 to the left and back. Do not stress the front panel panel ribbon cable.

4. Remove nine phillips screws holding left cover of A1. Remove left cover.

4.2.2 MODULES A1A4, A1A5, A1A5A1-A1A5A4

To gain access to A1A4, A1A5, or A1A5A1 through A1A5A4, proceed as follows:

1. Remove ten phillips screws holding right cover of A1.

2. Remove the right cover.

4.2.3 MODULE A2A1

To gain access to A2A1, proceed as follows:

1. Remove ten phillips screws holding left cover of A2.

2. Remove left cover.

4.3 PREVENTIVE MAINTENANCE

Preventive maintenance consists of visual inspection and cleaning. The procedures described in this paragraph are designed to improve the demodulator's reliability by preventing breakdowns and uncovering potential malfunctions before they impair the operation of the demodulator. Table 4-1 is a recommended schedule for performing preventive maintenance procedures.

Table 4-1. Preventive Maintenance Schedule

PROCEDURE	INTERVAL	COMMENTS
Cleaning	60 days	Interval variable depending on operating environment.
Inspection for damage	60 days	Interval variable depending on operating environment and equipment usage.
Performance Tests	180 days	Interval variable depending on operating environment and equipment usage.
Adjust/Alignment	-	Based on results of performance tests.

4.3.1 VISUAL INSPECTION

Many potential or existing faults can be detected by making a visual inspection of the unit. For this reason, a complete visual inspection should be made on a routine basis and whenever the demodulator is inoperative. At a minimum, the following items should be visually inspected:

1. Inspect the equipment covers and front panel for condition of finish and panel markings.
2. Inspect for dents, punctures, or warped areas.
3. Inspect quarter-turn fasteners and receptacles.
4. Inspect the external surfaces for loose or missing screws or washers.
5. Inspect the receptacles for conditions of pins, contacts, and mountings.
6. Inspect the internal components for signs of deterioration, discoloration or charring. Check for melted insulation and damaged, cracked, or broken components.

7. Inspect the printed circuit boards for damaged tracks, loose connections, corrosion, or other signs of deterioration.

8. Inspect the PC connectors, interface connectors, and chassis wiring for excessive wear, looseness, misalignment, corrosion, or other signs of deterioration.

4.3.2 CLEANING

Cleaning should be performed to remove accumulated dust and other contamination, and to ensure trouble-free operation.

CAUTION

Avoid the use of chemical cleaning agents containing bezene, toluene, zylene, acetone, or similar solvents. These chemicals may damage the plastics used in this demodulator.

1. Exterior - Dust the cabinet with a soft cloth. Dust the front panel controls with a small soft-bristled paint brush. Dirt clinging to the cabinet may be removed with a clean, lintfree cloth dampened with a mild detergent and water solution. Avoid using abrasive cleaners. They will scratch the front panel.

2. Interior - Dust in the interior of the unit should be removed before it builds up and causes arcing and short circuits during periods of high humidity. Dust is best removed by dry, low pressure air. Dirt clinging to surfaces may be removed with a soft-bristled paint brush or a clean, lint free cloth dampened with a mild detergent and water solution. Use a cotton tipped applicator for cleaning in narrow spaces and on the circuit boards.

4.4 DEMODULATOR PERFORMANCE TESTS

4.4.1 GENERAL

The performance tests outlined in this paragraph define the Minimum Performance Standards which ensure adequate demodulator functioning in all detection modes, gain modes, and IF bandwidths. The tests should be used for initial demodulator inspection, for preventive maintenance checks, for troubleshooting, or to varify demodulator performance after repairs have been made.

4.4.2 MINIMUM PERFORMANCE STANDARDS

Table 4-2 summarizes the parameters tested by the performance tests. To be acceptable for use, the demodulator should meet or exceed all minimum performance standards listed.

Table 4-2. Demodulator Minimum Performance Standards

PARAMETER TO BE TESTED	PERFORMANCE STANDARD
IF Gain, IF Input to IF Output	68 dB +/- 2 dB (150 kHz BW, IF Gain = Max)
Video Output, AM Mode	350 mVrms nominal into 75 ohms with rated input and 50% AM modulation at 400 Hz
Video Output, FM Mode	212 mVrms nominal into 75 ohms with rated input and 1/3 IF BW deviation at 400 Hz
Video Output, CW Mode	350 mV minimum into 75 ohms with rated input and 50% modulation at 400 Hz.
Video Output, Pulse Mode	1 v peak nominal into 75 ohms with rated input
Audio Output, all modes	1.25 Vrms into 600 ohms for 50% AM, FM 0.75 Vrms into 600 ohms, for peak deviation = 1/3 IF BW (all at rated input)
Signal to Noise Ratio (AM)	Greater than 10 dB with -94 dBm input and 150 kHz bandwidth
Dynamic Range	Maximum input signal with no distortion at least 60 dB above minimum rated input level
AGC Range, Peak Pulse and Average	Control range exceeds 50 dB with less than 2 dB output change
Manual Gain Control Range	Greater than 60 dB

4.4.3 TESTED EQUIPMENT REQUIRED

Table 4-3 lists the test equipment required for performance testing of the demodulator. Equivalent types of equipment may be used.

Table 4-3. Test Equipment Required

INSTRUMENT TYPE	RECOMMENDED INSTRUMENT
Equipment Frame	EFR100 Frame, with EPS100 Power Supply and IOM108 Interface Module
Signal Generator	HP8640B
Sweep Generator	HP8601
Pulse Generator	Systron-Donner 101D
Dual Trace Oscilloscope	Tektronix 475A
RF Voltmeter	Boonton 92B with 91-8B 50 ohm adaptor and high impedance probe tip
Digital Multimeter	HP3466A
AC Voltmeter	HP400FL
Termination Resistors (5)	75 ohm terminator, BNC connector 50 ohm terminator, BNC connector 10 K terminator, BNC connector 600 ohm terminator, BNC connector 5K resistor
Extender Cable	WJ Part No. 271408

4.4.4 PROCEDURE GUIDELINES

1. Read each test procedure thoroughly before attempting to perform test.

2. Hook up the proper test equipment as indicated in the test setup figure for each test.

3. Set the test equipment and demodulator controls as directed for each test.

4. Allow a minimum of 30 minutes warm-up time for test equipment prior to performing any of the tests.

5. Unless otherwise specified, acceptable tolerances are +/-3 dB for signal levels and +/-20% for ac and dc supply voltages.

6. The tests should be performed in the order given. If a malfunction is noted, refer to paragraph 4.5 for troubleshooting information.

4.4.5 IF GAIN TEST

1. Connect the demodulator as shown in Figure 4-1.

2. Using the front panel controls, set the demodulator to the following parameters:

   a. Bandwidth - 150 kHz
   b. Gain Mode - Manual
   c. IF Gain - Maximum clockwise
   d. Detection Mode - AM

3. Set the signal generator output frequency to 21.400 MHz CW, and set the output level to -88 dBm.

4. Set the RF voltmeter to -20 dBm range. The meter should indicate a minimum of -20 dBm +/-2dB.

5. Set the demodulator bandwidth to 500 kHz and the signal generator output level to -83 dBm. The RF voltmeter should indi- cate a minimum of -20 dBm +/-2 dB.

6. Set the demodulator bandwidth to 1 MHz and the signal generator output level to -80 dBm. The RF voltmeter should indi- cate a minimum of -20 dBm +/-2 dB.

7. Set the demodulator bandwidth to 4 MHz and the signal generator output level to -74 dBm. The RF voltmeter should indicate a minimum of -20 dBm +/-2 dB.

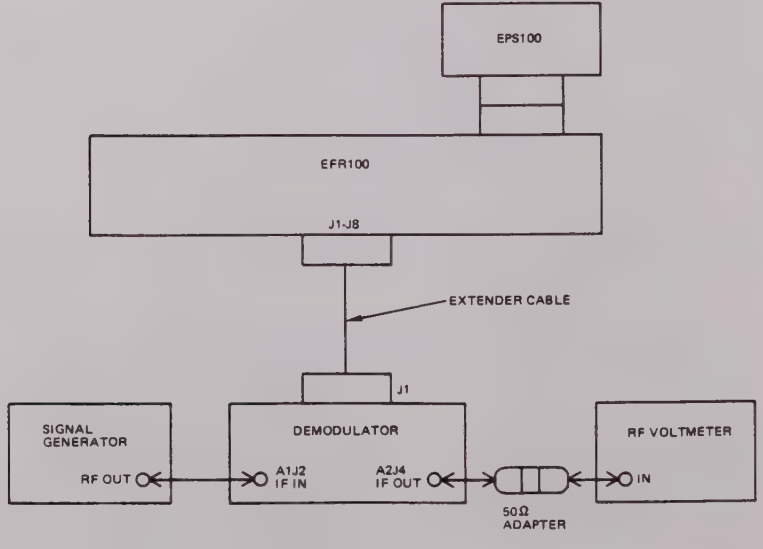


Figure 4-1. IF Gain Test Equipment Setup

4.4.6 VIDEO/AUDIO OUTPUT TEST

1. Connect the demodulator as shown in Figure 4-2.

2. Using the front panel controls, set the demodulator to the following parameters:

   a. Bandwidth - 150 kHz
   b. Gain Mode - AGC
   c. Detection Mode - AM

3. Set the oscilloscope settings to Dual Trace, .5V/DIV vertical, and 1 msec Hor. Time Base.

4. Set the signal generator output frequency to 21.400 MHz, AM 50% modulation, at 1 kHz rate, and set the output level to -88 dBm.

5. Channel A on oscilloscope should indicate a video signal of 1 V pp. Channel B should indicate an audio signal of 3V pp.

6. Set demodulator detection mode to CW.

7. Channel A on oscilloscope should indicate a video signal of 1V pp. Channel B should indicate an audio signal of 3 V pp.

8. Set the Signal generator output level to -74 dBm.

9. Set the oscilloscope to EXT. Trigger.

10. Set the pulse generator to provide a repetition rate of 1000 PPS and a pulse width of 100 usec. Adjust the output level for a 1.0 V positive pulse and adjust the pulse delay control to center the pulse on scope display.

11. On demodulator set bandwidth to 4 MHz and detection mode to Pulse.

12. Channel A on oscilloscope should indicate a video signal of 1 V pp. Channel B should indicate an audio signal of 3V pp.

13. Connect channel A input of oscilloscope to J6 of demodulator.

14. Set demodulator detection mode to FM, 150 kHz IF BW.

16. Set signal generator output level to -74 dBm and frequency to 21.4 MHz.

17. The oscilloscope should display approximately 0 Vdc. Rotate the IF BW control through the remaining 3 BW positions. The oscilloscope should display 0 Vdc in all BW positions.

18. Set demodulator bandwidth to 150 kHz. Manually offset the generator frequency by +75 kHz and -75 kHz. The oscilloscope should display +0.5 Vdc and -0.5 Vdc respectively.

19. Set demodulator bandwidth to 500 kHz. Manually offset the generator frequency by +250 kHz and -250 kHz. The oscilloscope should display +0.5 Vdc and -0.5 Vdc respectively.

20. Set the demodulator bandwidth to 1 MHz. Manually offset the generator frequency by +500 kHz and -500 kHz. The oscilloscope should display +0.5 Vdc and -0.5 Vdc respectively.

21. Set the demodulator bandwidth to 4 MHz. Manually offset the generator frequency by +2.5 MHz and -2.5 MHz. The oscilloscope should display +0.5 Vdc and -0.5 Vdc respectively.

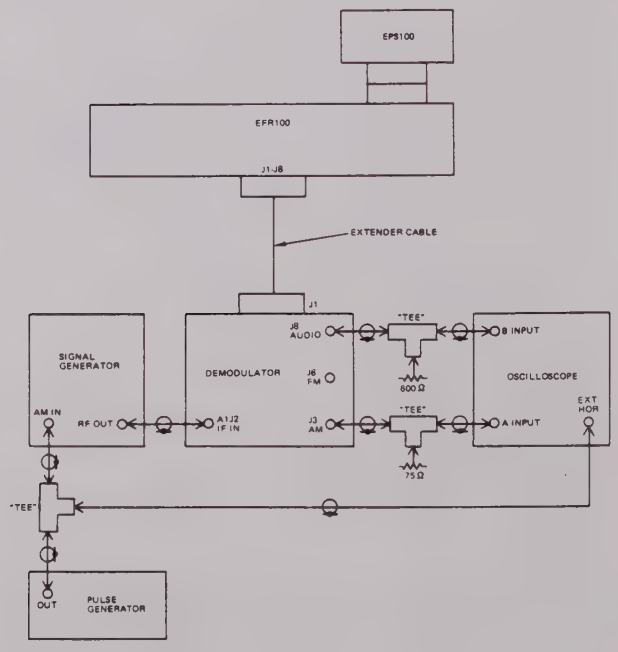


Figure 4-2. Video/Audio Output Test Setup

4.4.7 SIGNAL TO NOISE TEST

1. Connect demodulator as shown in Figure 4-3.

2. Using the front panel controls, set the demodulator to the following paramenters:

   a. Bandwidth - 150 kHz
   b. Gain Mode - Manual
   c. IF Gain - Maximum Clockwise
   d. Detection Mode - AM

3. Set signal generator to -94 dBm, 50% AM, 1 kHz rate and note reading.

4. Set the AC voltmeter to 1 Vrms range.

5. Remove modulation from signal generator.

6. The AC voltmeter should indicate a greater than 10dB decrease when modulation is turned off.

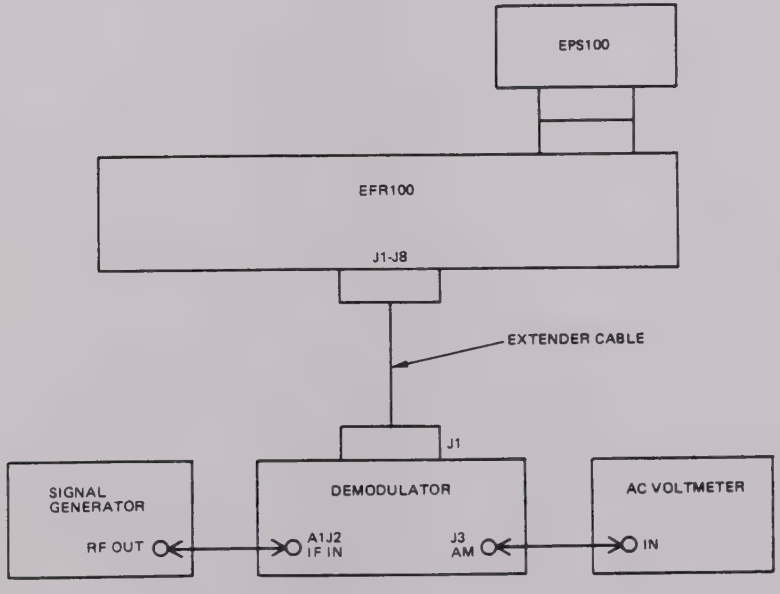


Figure 4-3. Signal to Noise Test Setup

4.4.8 DYNAMIC RANGE TEST

1. Connect demodulator as shown in Figure 4-4.

2. Using the front panel controls, set the demodulator to the following paramenters:

   a. Detection Mode - AM
   b. Gain Control - AGC

3. Set signal generator output frequency to 21.400 MHz, AM, and set the 50% modulation at 1kHz rate.

4. Set oscilloscope setting to .5V/DIV Vertical and 5 msec Hor. Time Base.

5. Measure the dynamic range of the demodulator in each band width using the AGC threshold levels listed in Table 4-4 by increasing the signal generator output level until distortion of video signal is observed on oscilloscope. The minimum level for distortion is the higher level indicated.

6. In each designated bandwidth the AM video output signal distortion shall not occur before maximum input signal level listed in Table 4-4.

Table 4-4. Dynamic Range Input Levels

BANDWIDTH	AGC THRESHOLD	MAXIMUM INPUT (No distortion)
150 kHz	-88 dBm	-38 dBm
500 kHz	-83 dBm	-33 dBm
1 MHz	-80 dBm	-30 dBm
4 MHz	-74 dBm	-24 dBm

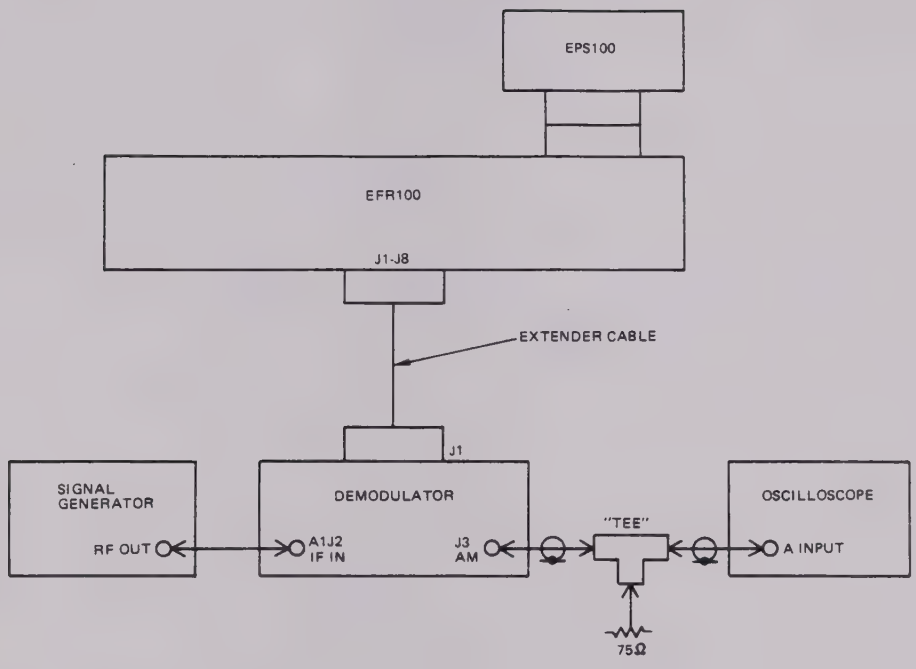


Figure 4-4. Dynamic Range Test Setup

4.4.9 GAIN CONTROL TEST

1. Connect equipment as shown in dotted lines on Figure 4-5.

2. Using the front panel controls, set the demodulator to the following parameters:

   a. Bandwidth - 4 MHz
   b. Gain Mode - AGC
   c. Detection Mode - Pulse

3. Set the signal generator output frequency to 21.400 MHz, CW, and set the output level to -74 dBm.

4. Set the oscilloscope to EXT. Trigger, .5V/DIV, and 5 msec Hor. Time Base.

5. Set the pulse generator to provide a repetition rate of 1000 PPS and a pulse of 100 usec. Adjust the output level for a 1.0 V positive pulse. Adjust the pulse delay control to center the pulse on scope display.

6. Connect equipment as shown in solid lines on Figure 4-5.

7. Observe pulse level on oscilloscope and increase the signal generator output level 50 dB higher.

8. The signal should change a maximum of 2 dB.

9. Connect equipment as shown in Figure 4-6.

10. Set the signal generator output frequency to 21.400 MHz, AM 50% modulation, at 1 kHz rate.

11. Set the demodulator to AM detection mode.

12. Set the bandwidth and input levels in accordance with Table 4-5. Measure the average levelling (output stability) on the AC voltmeter for each bandwidth of the demodulator.

13. The AGC control range should be 50 dB minimum and should maintain the output level change on AC voltmeter to 2 db maximum.

Table 4-5. Bandwidth and Input Level Settings

BANDWIDTH	INPUT LEVEL
150 kHz	-88 to -38 dBm
500 kHz	-83 to -33 dBm
1 MHz	-80 to -30 dBm
4 MHz	-74 to -24 dBm

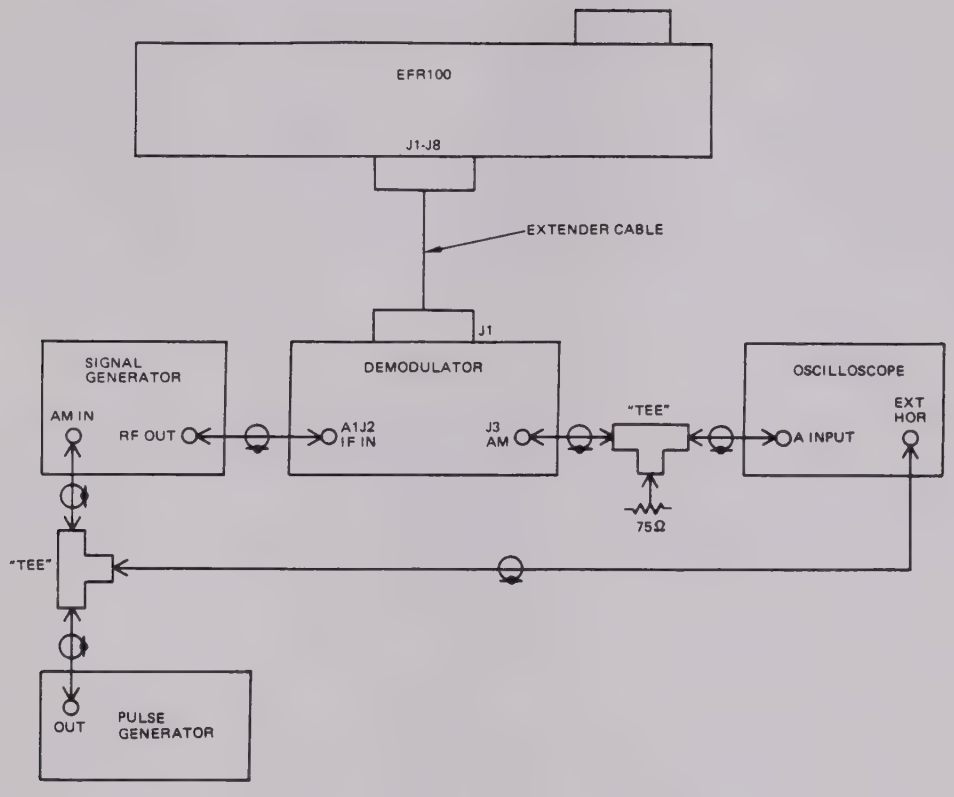


Figure 4-3. Gain Control Test Setup for Pulse Detection Mode

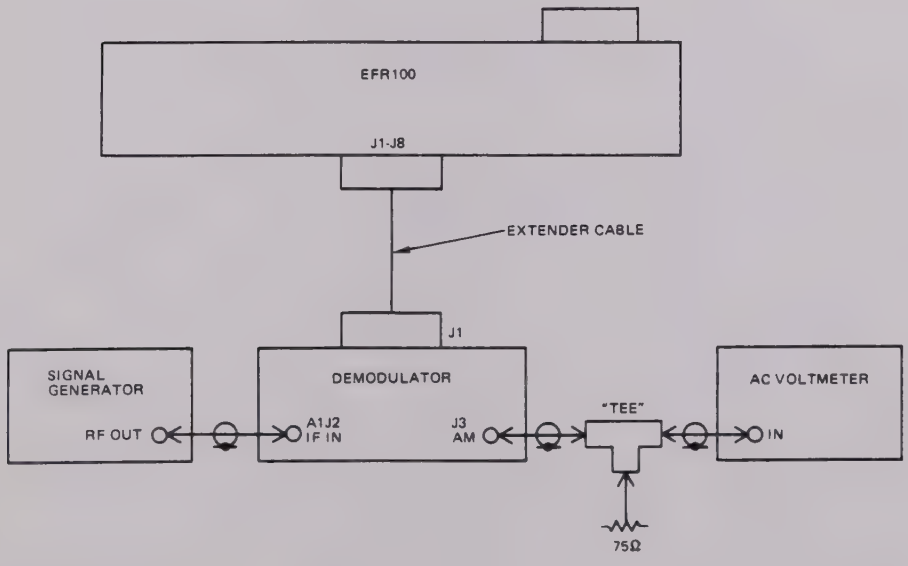


Figure 4-6. Gain Control Setup for AM Detection Mode

4.5 DEMODULATOR TROUBLESHOOTING PROCEDURES

4.5.1 GENERAL

Information is provided in this paragraph to troubleshoot the demodulator to isolate a defective replacable assembly or module. To locate a defective component on a module known to be defective, refer to paragraph 4.7 for individual module testing and troubleshooting. The demodulator will normally require troubleshooting as a result of failure to pass any of the performance tests in paragraph 4.4, or as a result of operator-observed malfunctions during normal operation.

4.5.2 TROUBLESHOOTING GUIDELINES

Table 4-6, IFD121 IF Demodulator Troubleshooting Chart, is provided as an aid in locating defective assemblies and modules within the modulator. Properly used, it is an effective guide to locating and correcting major demodulator failures. It is not intended as a substitute for standard signal tracing/fault isolation techniques performed by skilled technicians familiar with the demodulator circuitry.

1. Verify +18.3 Vdc at A1A1J1-1 and +8.2 Vdc at A1A1J1-3

2. Perform each of the performance tests in paragraph 4.4. Note any failure to achieve expected test results.

3. Refer to Table 4-6. Locate the performance test and fault symptom or symptoms noted in step 1.

4. Perform the additional tests and corrective action associated with the fault symptom. If a module is replaced and requires alignment, refer to paragraph 4.7 and perform the indicated alignment.

5. To confirm the corrective action, repeat the performance test in paragraph 4.4 that resulted in the fault symptom. Additional fault isolation may be required to locate the defective assembly or module.

6. The demodulator may be returned to service if it successfully passes all of the performance tests in paragraph 4.4.

7. Refer to paragraph 4.6 to repair any modules found defective after troubleshooting the demodulator.

Table 4-6. IFD121 IF Demodulator Troubleshooting Chart

PERFORMANCE TEST	FAULT SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
1. IF GAIN	No gain in any BW	Defective A1A1	Increase input signal to -40 dBm. Check at A1A1E3, E4. Should be 230 mV. If not good, check A1A1P2-4 for +13 Vdc. Also check A1A1P1 for 100 mVdc. If all readings are good, replace A1A1.
		Defective A1A2	Check signal at A1A2E3 with signal generator set to -88 dBm. Should be 63.7 mVpp. If not good, check A1A2P2-9 for +5 Vdc and A1A2P2-11 for 0 Vdc. If both are good, replace A1A2.
	No gain in one or more BW's	Defective IF Filter	Check A1A1E4 as above. If signal is good on all BW's, replace A1A2. If not good, replace A1A1.
	If filter switching does not appear to occur.	Defective BW Select Code.	Check BW Select Code at A1A2P2-4, 5 and continuity to A1A1J1-5,6. If not good, check front-panel BW switch. If switch is good, replace A1A4.
2. VIDEO/ AUDIO OUTPUT	No AM video in AM Mode.	Defective A1A2	Check A1A2P3 for 0.5 Vpp at 400 Hz. If not good, check A1A2J2-7 for 5 Vdc If not good, check front panel mode switch. If switch is good, replace A1A4. Otherwise replace A1A2.

Table 4-6. IFD121 IF Demodulator Troubleshooting Chart

PERFORMANCE TEST	FAULT SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
2. VIDEO/ AUDIO OUTPUT (cont'd)		Defective A1A5	Check A1A2P2 for 0.5 at 400 Hz. If not good replace A1A5. If good check for 0.5 Vpp at A1A3J2-1. If bad, check cable.
		Defective A1A3	Check A1A3E2, E7 for 1 Vpp at 400 Hz. If not good, replace A1A3.
	No AM video in CW mode.	Defective A1A2	Check A1A2J2-7 for 0 Vdc. If good, replace A1A2. If not good, check front panel mode switch. If switch is good, replace A1A4.
	No FM video	Defective A1A5 or cable assembly	Check A1A5P1 for 0.5 Vpp at 400 Hz. Check for 0.5 Vpp at A1A3J2-4. If bad, check assembly. If good, replace A1A3. If not good, replace A1A5 or A1A5A1-A1A5A4.
		Defective A1A2	Check A1A5P4 for presence of 21.4 MHz (-20 dBm). If not good, place A1A2.
	No sel. audio	Defective A1A3	Replace A1A3
3. S/N RATIO	Signal noise is less than 10 dB	Improper IF gain alignment.	Perform IF gain alignment per paragraph 4.7.2
		Excessive loss in demodulator front end.	Replace A1A1.
4. DYNAMIC RANGE	Distortion occurs before end of dynamic range.	Defective A1A1	Check A1A1E3 for distortions of modulation envelope. If distortion occurs, check A1A1P2-4 for +3 Vdc. If good, replace A1A1. If not good, replace A1A2

Table 4-6. IFD121 IF Demodulator Troubleshooting Chart

PERFORMANCE TEST	FAULT SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
5. GAIN CONTROL	Gain control range is less than 50 dB.	Defective A1A1 or A1A2	Check A1A1P2-7 for +3 Vdc under maximum signal. If good, check A1A2Q5 emitter for -3.7 Vdc. If not present replace A1A2. If not good replace A1A2.
		Defective A1A2	Check A1A2P2-9 for 0 Vdc. If good replace A1A2 . If not good, check front panel MAN/AGC switch. If switch is good, replace A1A4.
		Defective IF GAIN control (MAN mode only)	Set manual gain control max. CCW. Check A1J2-4 for +3 Vdc. If not good, replace A1A4. Check A1J2-5 for 0 to +5 Vdc swing. If not good, replace R1. Otherwise replace A1A4.

4.6 MODULE TESTING AND REPAIR PROCEDURES

4.6.1 GENERAL

This paragraph provides the testing, troubleshooting, and repair information necessary to restore a malfunctioning module to normal operation. The information provided consists of the following categories:

1. Module test and troubleshooting procedures to assist signal tracing and localize faulty circuit areas.

2. Fault isolation tables to assist isolating defective components in faulty circuit areas. Semiconductor voltage tables provided to assist locating faulty transistors and integrated circuits.

3. A Parts Replacement Guide, paragraph 4.6.9, is provided to assist in repairing a defective module.

4.6.2 PROCEDURE GUIDELINES

The module testing and troubleshooting procedures are defined using an EFR100 Equipment Frame, EPS100 Power Supply, and an IOM108 I/O Module as a demodulator test bed. Figure 4-7 is a block diagram showing the test bed configuration which will be used in each of the module testing and troubleshooting procedures. If a different hardware configuration is being utilized, it will be necessary to supply the proper dc power to J1 on the demodulator rear panel. The dc power supply requirements are listed in Table 4-7.

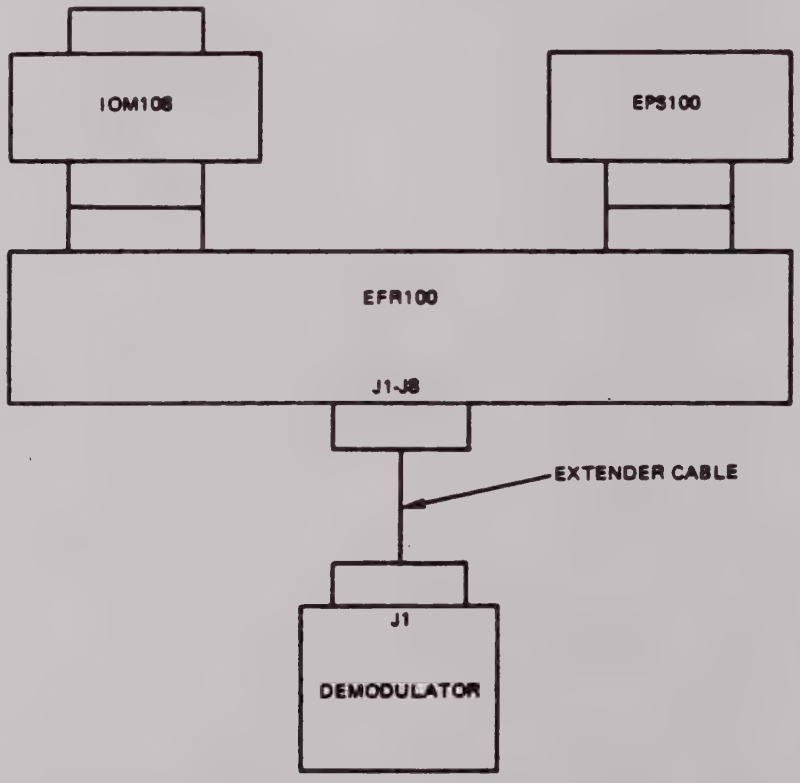


Figure 4-7. Demodulator Module Test Configuration

Table 4-7. Demodulator Rear Panel DC Requirements

J1-6	+29 Vdc
J1-7	+18 Vdc
J1-19	-18 Vdc
J1-20	+ 8 Vdc

When testing and troubleshooting a defective module, observe the following guidelines:

1. Allow the test equipment a 30 minute warm-up before any test is performed.

2 Refer to the testing and troubleshooting paragraph for the desired module. Configure the demodulator and test equipment as indicated in the test procedure for the module.

3. Perform the testing and troubleshooting procedure in the sequence given. If any failure is encountered or any desired result is not obtained, the Fault Isolation Table lists which key components would most likely cause the failure.

4. Refer to paragraph 4.6.9, Parts Replacement Guide, and replace the key components indicated in step 3 above. Repeat Testing and Troubleshooting Procedure to confirm the corrective action.

5. If the module still fails, additional troubleshooting and signal tracing is required. Refer to the circuit descriptions in Section III and schematic diagrams in Section VI as aids in performing additional troubleshooting.

4.6.3 21.4 MHZ BANDPASS AMPLIFIER, A1, TESTING AND TROUBLESHOOTING

This paragraph describes the procedures to test, troubleshoot and repair the 21.4 MHz Bandpass Amplifier.

A signal generator and an RF voltmeter (see Table 4-3) are required to perform the tests outlined in the following paragraphs.

4.6.3.1 Preliminary Setup Procedure

The following preliminary setup steps should be performed prior to testing or troubleshooting the 21.4 MHz Bandpass Amplifier:

1. Deenergize the demodulator.

2. Remove the demodulator from the equipment frame (see paragraph 2.3.1 for details.)

3. Refer to paragraph 4.2 and use the procedure given to provide access to module A1A1.

4. Interconnect J1 on the demodulator rear panel with its mating connector on the equipment frame using the appropriate extender cable (see Figure 4-7.)

5. Connect the signal generator RF output to demodulator rear panel IF input jack, A1J2, using a coaxial cable, BNC to SMA connectors.

6. Set the signal generator as follows:

   a. RF Frequency -- 21.4 MHz
   b. Output Level -- 20 dBm
   c. Modulation -- None

7. Energize the demodulator using the power switch on the equipment frame power supply. Set the demodulator front panel controls as follows:

   a. LOCAL/REMOTE -- LOCAL
   b. MAN/AGC -- MAN
   c. IF GAIN -- Max. CW
   d. DET. MODE -- AM
   e. EF BW -- 4 MHz

8. Using the RF Voltmeter probe tip, verigy that a 23 mV signal at 21.4 MHz is present at A1E1.

4.6.3.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information in this paragraph is keyed to Table 4-8, 21.4 MHz Bandpass Amplifier Fault Isolation Table. This chart is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure in paragraph 4.6.3.1.

2. Using an RF Voltmeter and high impendance probe tip, check each test point listed in Table 4-8. Where indicated, observe special instructions in the comments column.

3. When a faulty signal is encountered, replace they key components indicated in Table 4-8. Paragraph 4.6.9, Parts Replacement Guide, should be referred as an aid in removing and replacing any PCB components.

4. Replacement of the indicated key components will normally restore the faulty test point signal to normal. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to Table 4-9, 21.4 MHz Bandpass Amplifier Semiconductor Voltage Table, and Figure 6-1, 21.4 MHz Bandpass Amplifier Schematic Diagram for additional aid in troubleshooting.

Table 4-8. 21.4 MHz Bandpass Amplifier Fault Isolation Table

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
E1	23 mV at 21.4 MHz	Input cables	
E3	60 mV	U1, U2	
U4-4	145 mV	U3, U4	Check voltage at U3-3. Should be +13 vdc (2nd IF agc)
CR1 cath.	225 mV	T1	
CR9 cath.	100 mV all BW's	FL1-FL4, CR1-CR12, U6	Verify correct BW code input at J1-5,6
U9-7	50 mV (with input reduced to -40 dBm)	U9	Check again adjust voltage at U9-2,3. Should be approx. +100 mV on all BW's

Table 4-9. 21.4 MHz Bandpass Amplifier Semiconductor Voltage Table

DEVICE	PIN	VOLTAGE	DEVICE	PIN	VOLTAGE
U1	1	+15 V	U3	1	+13 V
	2	0 V		2	+15 V
	3	0 V		3	0 V
	4	0 V		5	0 V
U4	1	+15 V	U5	1	+15 V
	2	0 V		3	+18 V
	4	0 V			
U6	3	+15 V	U7	1	+15 V
	13	+15 V		3	+18 V
	16	+15 V			
	9,10	0 or +5 V (BW code)			
	1,2,4, 5,11,12 14,15	0 or +15 V (Filter select)			
U8	1	+5 V	U9	2,3	100 mV
	2	+6.5 V		7	0 V
	3	+8.2 V		8	+6.5 V

4.6.4 AM/SSB/CW DEMODULATOR, A1A2, TESTING AND TROUBLESHOOTING

This paragraph describes the procedure to test, troubleshoot and repair the AM/SSB/CW Demodulator. A signal generator, RF Voltmeter and an oscilloscope (see Table 4-3) are required to perform the tests outlined in the following paragraphs:

4.6.4.1 Preliminary Setup Procedure

The following preliminary setup steps should be performed prior to testing or troubleshooting the AM/SSB/CW Demodulator.

1. Deenergize the demodulator
2. Remove the demodulator from the equipment frame (see paragraph 2.3.1 for details.)
3. Refer to paragraph 4.2 and use the procdure given to provide access to module A1A2.
4. Interconnect J1 on the demodulator rear panel with its mating connector on the equipment frame using the appropriate extender cable (see Figure 4-7.)
5. Connect the signal generator RF output to demodulator rear panel IF input jack, A1J2, using a coaxial cable, BNC to SMA connectors.
6. Energize the demodulator using the power switch on the equipment frame power supply.

4.6.4.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information in this paragraph corresponds to Table 4-10, AM/SSB/CW Demodulator Fault Isolation Table IF section, and Table 4-11, AM/SSB/CW Demodulator Fault Isolation Table AGC section. These charts are used to isolate the module fault to a defective stage or circuit. Testing and Troubleshooting of the AM/SSB/CW Demodulator consists of two different procedures: One procedure for the IF section and one procedure for the AGC section. These procedures may be performed independently, although it is advised to verify proper IF section operation before performing the AGC section procedure.

4.6.4.2.1 IF Section Testing and Troubleshooting Procedure.

Perform the following procedures in the sequence given;

1. Perform the preliminary setup procedure in paragraph 4.6.4.1.

2. Set the generator signal as follows:

   a. RF Frequency -- 21.400 MHz
   b. Output Level -- -30 dBm
   c. Modulation -- Modulation requirement stated in Table 4-10.

3. Set the demodulator front panel controls as follows:

   a. LOCAL/REMOTE -- LOCAL
   b. MAN/AGC -- MAN
   c. IF GAIN -- Max. CW
   d. DET. MODE -- Detection Mode requirements stated in Table 4-10.
   e. IF BW -- 4 MHz

4. Using the RF probe tip on RF voltmeter, verify that approximately a 360 mV signal at 21.4 MHz is present at A2R9.

5. Using an RF voltmeter probe tip or oscilloscope where indicated, check each test point listed in Table 4-10. Where indicated observe special instruction in the comments column. When a faulty signal is encountered, replace the key components indicated in Table 4-10. Paragraph 4.6.9, Parts Replacement Guide should be referred to as an aid in removing any PCB components.

6. Replacement of the indicated key components will normally restore the faulty test point signal to normal. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to Figure 6-2, AM/SSB/CW Demodulator Schematic Diagram for additional aid in troubleshooting.

4.6.4.2.2 AGC Section Testing and Troubleshooting Procedure

Perform the following procedures in the sequence given:

1. Perform the preliminary setup in paragraph 4.6.4.1

2. Set the signal generator as follows:

   a. RF Frequency -- 21.400 MHz
   b. Output Level -- -20 dBm
   c. Modulation -- None

3. Set the demodulator front panel controls as follows:

   a. LOCAL/REMOTE -- LOCAL
   b. MAN/AGC -- AGC
   c. IF GAIN -- N/A
   d. DET. MODE -- AM
   e. IF BW -- 4 MHz

4. Using the oscilloscope test probe, verify that a +0.5 Vdc signal is present at U4-6.

5. Using an oscilloscope and high impedance compensated probe, check each test point listed in Table 4-11. Where indicated, observe special instruction in the comments column. Note that the test point data is presented for conditions of signal present and no signal present. When a faulty signal is encountered, replace the key components indicated in Table 4-11. Paragraph 4.6.9, Parts Replacement Guide, should be referred to as an aid in removing and replacing any PCB components.

6. Replacement of the indicated key components will normally restore the faulty test point signal to normal. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessry. Refer to Figure 6-2, AM/SSB/CW Demodulator Schematic Diagram for additional aid in troubelshooting.

Table 4-10. AM/SSB/CW Demodulator Fault Isolation Table, IF Section

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
Q1-3	360 mv at 21.4 MHz	Input Cabling, T1	No moulation, CW Mode
Q1-1	1.5 V	Q1	Input Level = -50 dBm
AT1-5	200 mV	C8, C9, C10, L4	
U2-1	30 mV	AT1	Level depends on setting of AT1.
CR6-anode	500 mV (4 MHz) 900 mV (1 MHz) 1100 mV (500 kHz) 800 mV (150 kHz)	CR2-CR7, U3A	Rotate BW switch through all BW positions. Input= -70 dBm

Table 4-10. AM/SSB/CW Demodulator Fault Isolation Table, IF Section (Cont'd)

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
U4-3	+0.5 Vdc	T1, C33, CR8	Use Oscilloscope
U4-6	+1.0 Vdc	U4	Use Oscilloscope
U5-1	90 mV	T3	Input Level=-50 dBM
P4	140 mV	U1	
U6-10	600 mV	Q4, Y1	BFO Signal. Only present in CW mode.
U6-12	1.7 V at 400 Hz	U6	Change Signal Generator to 21.4004 MHz. Use Oscilloscope.
U7-1	3.0 V	U7	Use Oscilloscope.

Table 4-11. AM/SSB/CW Demodulator Fault Isolation Table, AGC Section

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
U1-13	+2 Vdc **	U1	
U4-6	+0.5 Vdc	IF Section	See Table 4-10.
U7-14	+0.5 Vdc	U7, U11, CR9, CR 16	
U7-8	+1 Vdc * -2.6 Vdc**	U7, U8, CR 10	
U10-8	-1 Vdc * +2.6 Vdc **	U3, U10	
Q5-E	0 Vdc *	U10, Q5	
U10-1	+15 Vdc * - 6 Vdc **	U10	
U7-7	+14 Vdc * +2.5 Vdc **	U7, CR12, CR15	
U10-7	-14 Vdc * +8 Vdc **	U10, CR14	

* No input signal
** Input signal = -20 dBm

Table 4-12. AM/SSB/CW Demodulator Semiconductor Voltage Table

DEVICE	PIN	VOLTAGE	DEVICE	PIN	VOLTAGE
Q1	1	+15 V	Q2	E	+14.8 V
	2	+ 4 V		B	+14 V
	3	+ 2 V		C	+0.2 V
	4	+ 1 V			
Q3	E	+5.6 (full sig.)	Q4	E	+2 V
	B	+5		B	+2.5 V
	C	0		C	+15 V
Q5	E	-3.7 (full sig.)	U1	1	+6.5 V
	B	-4.5		12	+3 V
	C	0		13	+2 V (full sig.)
U2	1	0	U4	1	+15 V
	2	+6.5		2	+0.5 V (full sig.)
	3	0		3	+0.5 V (full sig.)
				6	+0.5 V (full sig.)
U5	1	0		4	-15 V
	2	+6.5 V		5	+15 V
	3	0		7	+15 V
U6	1	+5 V	U7	1	0
	4	+5 V		2	0
	5	+1 V		3	0
	6	+7 V		4	+15 V
	8	+10 V		5	+14 V (no sig.)
	12	+7 V		6	+14 V (no sig.)
				7	+14 V (no sig.)
U15	1,2,6,8,	+15 V		8	+1 V (no sig.)
	12,12,14			9	+0.04 (no sig.)
	4,10	0 (no sig.)		10	+0.04 (no sig.)
	5,7	0		11	-15 V
	9	Short + spike		12	0 (no sig.)
		200 ms after		13	0 (no sig.)
		signal turnoff.		14	0 (no sig.)
U10	1	+15 V (no sig.)	U11	2	0 (no sig.)
	2	+1.5 V (no sig.)		3	0 (no sig.)
	3	+2 V (no sig.)		4	-15 V
	4	+15 V		6	0 (no sig.)
	5	-1 V (no sig.)		7	+15 V
	6	+2 V			
	7	-14 V (no sig.)	U12	1	+15 V
	8	-1 V (no sig.)		3	+18 V
	9	0			
	10	0	U13	1	-15 V
	11	+15 V		3	-18 V
	12	0	U14	1	+1.2 V
	13	0		2	+6.5 V
	14	+2 V (no sig.)		3	+8.2 V

4.6.5 VIDEO/AUDIO, A1A3, TESTING AND TROUBLESHOOTING

This paragraph describes the procedures to test, troubleshoot and repair the Video/Audio, A1A3. A signal generator and an oscilloscope (see Table 4-3) are required to perform the tests outlined below.

4.6.5.1 Preliminary Setup Procedure

The following preliminary setup steps should be performed prior to testing or troubleshooting the Video/Audio:

1. Deenergize the demodulator

2. Remove the demodulator from the equipment frame (see paragraph 2.3.1 for details.)

3. Refer to paragraph 4.2 and use the procedure given to provide access to module A1A3.

4. Interconnect J1 on the demodulator using rear panel with its mating connect or on the equipment frame using the appropriate extender cable (see Figure 4-7.)

5. Connect the signal generator RF output to demodulator rear panel IF input jack, A1J2, using a coaxial cable, BNC to SMA connectors.

6. Set the signal generator as follows:

   a. RF Frequency -- 21.4 MHz
   b. Output Level -- -70 dBm
   c. Modulation -- 50% AM

7. Energize the demodulator using the power switch on the equipment frame power supply. Set the demodulator front panel controls as follows:

   a. LOCAL/REMOTE -- LOCAL
   b. MAN/AGC -- AGC
   c. IF GAIN -- Max. CW
   d. DET. MODE -- AM
   e. IF BW -- 150 KHz

4.6.5.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information in this paragraph corresponds to Table 4-13, Video/Audio Fault Isolation Table. This chart is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given:

1. Perform the preliminary setup procedure in paragraph 4.6.5.1.

2. Using an oscilloscope and a high impedance compensated probe, check each test point listed in Table 4-13. Where indicated, observe special instructions in the comments column.

3. When a faulty signal is encountered, replace the key components indicated in Table 4-13. Paragraph 4.6.9, Parts Replacement Guide, should be referred to as an aid in removing and replacing PCB components.

4. Replacement of the indicated key components will normally restore the faulty test point signal to normal. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to Table 4-14, Video/Audio Semiconductor Voltage and Figure 6-3, Video, Audio Schematic Diagram for additional aid in troubleshooting.

Table 4-13. Video/Audio Fault Isolation Table

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
U2-3	0.25 Vpp at 400 Hz	Input cabling	AM mode with 50% AM
U2-6	2.25 Vpp	U2	
U11-8	2.0 Vpp	U11	
U12-8	2.0 Vpp	U12	
J2-4	0.25 Vpp at 400 Hz	Input cabling	FM mode with 1/3 IF BW deviation at 400 Hz.
U1-6	1.35 Vpp	U1	
U5-8	1.2 Vpp	U5	
U7-8	1.2 Vpp	U7	
U4-6	7 Vpp (AM mode) 4.3 Vpp (FM mode)	U3, U4	
U10-3	0 V * +1 V **	Input cabling	
U10-6	0 V * +1 V **	U10, CR1	

TABLE 4-13 (CONT'D)
TABLE 4-14

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
U6-8	0 V *V	Input cabling	
U6-14	0 V * +1 V **	CR2, U6	
U6-1	-13 V * +13 V **		
U6-7	0 V * +4 V **		

* No Signal
** Input Signal = -70 dBm

Table 4-14. Video/Audio Semiconductor Voltage Table

DEVICE	PIN	VOLTAGE	DEVICE	PIN	VOLTAGE
U1	2,3,6	0 (No signal)	U2	2,3,6	0 V (no signal)
	4	-15 V		4	-15 V
	7	+15 V		7	+15 V
U4	2,3,6	0 V	U5	3,8	0 V (no signal)
	4	-15 V		1,2	+15 V
	7	+15 V		4,5	-15 V
U6	1	-13 V (no sig.)	U7	3,8	0 V (no signal)
	2	+1.5 V		1,3	+15 V
	3	+1.5 V		4,5	-15 V
	4	+15 V			
	5	0	U8	2	-18 V
	6	0		3	-15 V
	7	+1 V (no sig.)			
	8	0 (no sig.)	U9	1	+18 V
	9	0 (no sig.)		2	+15 V
	10	0 (no sig.)			
	11	-15 V	U10	2	0 V (no signal)
	12	0		3	0 V (no signal)
	13	0		4	-15 V
	14	-1 V (no sig.)		6	0 V (no signal)
				7	+15 V
U11	3,8	0 V (no sig.)	U12	3,8	0 V (no signal)
	1,2	+15 V		1,2	+15 V
	4,5	-15 V		4,5	-15 V
U13	2	-18 V			
	3	-15 V			

4.6.6 FM DEMODULATOR, A1A5, TESTING AND TROUBLESHOOTING

This paragraph describes the procedures to test, troubleshoot, and repair the FM demodulator, A1A5, and FM demodulator modules, A1A5A1 through A1A5A4. A signal generator, RF voltmeter, and an oscilloscope (see Table 4-3) are required to perform the tests outlined below.

4.6.6.1 Preliminary Setup Procedure

The following preliminary setup steps should be performed prior to testing or troubleshooting the FM demodulator.

1. Deenergize the demodulator.

2. Remove the demodulator from the equipment frame (see paragraph 2.3.1 for details.)

3. Refer to paragraph 4.2 and use the procedure given to provide access to module A1A5.

4. Interconnect J1 on the demodulator rear panel with its mating connector on the equipment fram using the appropriate extender cable (see Figure 4-7.)

5. Connect the signal generator RF output to demodulator rear panel IF input jack, A1J2, using a coaxial cable, BNC to SMA connectors.

6. Set the signal generator as follows:

   a. RF Frequency -- 21.4 MHz
   b. Output Level -- -70 dBm
   c. FM Modulation -- Deviation = 1/3 IF BW, 400 Hz rate.

7. Energize demodulator using the power switch on the equipment frame power supply. Set the demodulator front panel controls as follows:

   a. LOCAL/REMOTE -- LOCAL
   b. MAN/AGC -- MAN
   c. IF GAIN -- Max. CW
   d. DET. MODE -- FM
   e. IF BW -- 150 kHz

8. Using the RF voltmeter probe tip verify that a 20 mv rms signal at 21.4 MHz is present at A5P4.

4.6.6.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information in this paragraph corresponds to Table 4-15, FM Demodulator Motherboard Fault Isolation Table, Table 4-16, Wideband FM Demodulator Module Fault Isolation and Table, 4-17, Narrowband FM Demodulator Fault Isolation Table. These charts are used to isolate the FM demodulator fault to a defective stage or circuit.

Perform the following procedures in the sequence given:

1. Perform the preliminary setup procedure in paragraph.

2. Using an RF voltmeter RF probe tip or oscilloscope where indicated, check each test point listed in Table 4-15. Where indicated, observe special instructions in the comments column.

3. When a faulty signal is encountered, replace the key components indicated in Table 4-15. Paragraph 4.6.9, Part Replacement Guide, should be referred to as an aid in removing and replacing any PCB components.

4. If Table 4-15 indicates a faulty FM demodulator module, A5A1A1 through A5A1A4, the module fault may be confirmed by removing it and substituting one of the other three modules in its place. Once the module is confirmed as faulty, refer to either Table 4-16, Wideband FM Demodulator Module Fault Isolation Table. Use the oscilloscope and high impedence compensated probe to check each test point listed in the appropriate table. When a faulty signal is found on the FM demodulator module, replace the key components indicated in the fault isolation table. Paragraph 4.6.9, Parts Replacement Guide, should be referred to as an aid in removing any PCB components.

5. Replacement of the indicated key components will normally restore the faulty test point signal to normal. If a faulty signal is still observed after key components replacement, additional signal tracing/fault isolation is necessary. Refer to the following tables and figures for additional aid in troubleshooting: Table 4-18, FM Demodulator Motherboard Semiconductor Voltage Table, Table 4-19, Wideband FM Demodulator Module Semiconductor Voltage Table, or Table 4-20, Narrowband FM Demodulator Semconductor Voltage Table and Figure 6-5, FM Demodulator Motherboard Schematic Diagram, Figure 6-6, FM Demodulator (25-300 kHz) Schematic Diagram or Figure 6-7, FM Demodulator (300 kHz - 4 MHz) Scematic Diagram.

Table 4-15. FM Demodulator Motherboard Fault Isolation Table

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
P4	20 mVrms min. at 21.4 MHz	Input cabling	Use RF voltmeter probe
A1P1-11	+15 V	U1, U2	When BW1 is selected
A2P1-1	-15 V	U1, U2	" "
A2P1-11	+15 V	U1, U2	When BW2 is selected
A2P2-1	-15 V	U1-U2	" "
A3P1-11	+15 V	U2-U3	When BW3 is selected
A3P2-1	-15 V	U2-U3	" "
A4P1-11	+15 V	U2-U3	When BW4 is selected
A4P2-1	-15 V	U2, U3	" "
U5-1	0.6 Vpp at 400 Hz *	A1	BW1
U5-5	0.6 Vpp at 400 Hz *	A2	BW2
U5-2	0.3 Vpp at 400 Hz **	A3	BW3
U5-4	0.5 Vdc ***	A4	BW4
U5-3	0.6 Vpp at 400 Hz *	U5	For BW1 and BW2
U6-6	0 Vdc	U6	No modulation IF=21.4 MHz
U4-13	0.25 Vpp at 400 Hz	U4	Select AM mode. Set generator for 50% AM at 400 Hz.
U2-3	100 mVdc (Gain Set)	U2, A1-A4 (BW1-BW4)	Rotate BW select switch through all BW's.

* FM Deviation = 1/3 IF bandwidth
** FM Deviation = 150 kHz peak
*** No FM Modulation. Signal generator frequency = 23.4 MHz

Table 4-16. Wideband FM Demodulator Fault Isolation Table

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
U1-1	20 mV at 21.4 MHz at 21.4 MHz	Input cabling	Use RF voltmeter probe
U1-5	0.7 V at 21.4 MHz	U1	Use RF voltmeter probe
U2-6	0.6 Vpp at 400 Hz. *	CR 1, CR 2, U2	For 500 kHz BW
P1-4,5,6, 7,8	BW ID Code	CR 3-CR7	See Paragraph 3.3.1.4.1 for specific BW ID code values
U2-6	0.3 Vpp at 400 Hz **		For 1 MHz BW
U2-6	0.5 Vdc		For 4 MHz BW

* FM Deviation = 1/3 IF Bandwidth for 500 kHz BW.
** FM Deviation = 150 kHz
*** No FM Modulation. Signal Generator = 23.4 MHz

Table 4-17. Narrowband FM Demodulator Fault Isolation Table

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
U1-1	20 mv at 21.4 MHz	Input cabling	
C6	1.5 V at 21.4 MHz	U1, R2	
U2-14	0.6 Vpp at 400 Hz *	U2	
P1-4,5,6, 7,8	BW ID Code	CR3-CR7	See paragraph 3.3.1.4.1 for specific BW ID code values

* FM Deviation = 1/3 IF Bandwidth

Table 4-18. FM Demodulator Motherboard Semiconductor Voltage Table

DEVICE	PIN	VOLTAGE	DEVICE	PIN	VOLTAGE
U1	2,13,14	+15 V	U2	13,16	+15 V
	5,8,9,10	-15 V		11,12	+15 V (when
	6,9	+15 (when selected)		14,15	selected)
	3,12	+15 (when selected)		9,10	BW select input (0 or +5 Vdc)
	4,11	-15 (when selected)			
U3	2,13,14	+15 V	U4	7	+10 V
	5,8,10	-15 V		9,10	BW select input (0 or +5 Vdc)
	6,9	+15 (when selected by U2)		16	+10 V
	3,12	+15 (when selected)			
	4,11	-15 (when selected)			
U5	7	+10 V	U6	1	+15 V
	9,10	BW select input (0 or +5 Vdc)		2	0 V
				3	0 V
	16	+10 V		4	-15 V
				5	+15 V
				6	0 V(no sig.)
				7	+15 V
U7	1	+15 V	U8	2	-18 V
	3	+18 V		3	-15 V

Table 4-19. Wideband FM Demodulator Semiconductor Voltage Table

DEVICE	PIN	VOLTAGE	DEVICE	PIN	VOLTAGE
U1	1	+3 V	U2	1	+15 V
	2	+3 V		2	0 V (no signal)
	3	+3 V		3	0 V (no signal)
	4	+2.5 V (no signal)		4	-15 V
	5	+7 V		5	+15 V
	10	+10 V		6	0 V (no signal)
				7	+15 V

Table 4-20. Narrowband FM Demodulator Semiconductor Voltage Table

DEVICE	PIN	VOLTAGE	DEVICE	PIN	VOLTAGE
U1	1	+3 V	U2	1	0 (no signal)
	2	+3 V		2	0 (no signal)
	3	+3 V		3	0 (no signal)
	4	+2.5 V (no sig.)		4	+15 V (no signal)
	5	+7 V		5	5 (no signal)
	10	+10 V		6	6 (no signal)
				7	7 (no signal)
				11	-15 V
				12	0 (no signal)
				13	0 (no signal)
				14	0 (no signal)

4.6.7 WIDEBAND IF AMPLIFIER, A2A1, TESTING AND TROUBLESHOOTING

This paragraph describes the procedures to test, troubleshoot and repair the wideband IF amplifier. A signal generator and an RF voltmeter (see Table 4-3) are required to perform the tests outlined below.

4.6.7.1 Preliminary Setup Procedure

The following preliminary setup steps should be performed prior to testing or troubleshooting the wideband IF amplifier:

1. Deenergize the demodulator.

2. Remove the demodulator from the equipment frame (see paragraph 2.3.1 for details.)

3. Refer to paragraph 4.2 and use the procedure given to provide access to module A2A1.

4. Interconnect J1 on the demodulator rear panel with its mating connector on the equipment frame using the appropriate extender cable (see Figure 4-7.)

5. Connect the signal generator RF output to demodulator rear panel IF input jack, A1J2, using a coaxial cable, BNC to SMA connectors.

6. Set the signal generator as follows:

    a. RF Frequency -- 21.4 MHz
    b. Output Level -- -20 dBm
    c. Modulation -- None

7. Energize the demodulator using the power switch on the equipment frame power supply. Set the demodulator front panel controls as follows:

   a. LOCAL/REMOTE -- LOCAL
   b. MAN/AGC -- MAN
   c. IF GAIN -- Max. CW
   d. DET. MODE -- AM
   e. IF BW -- 4 MHz

8. Using the RF voltmeter probe tip, verify that a 58 mv rms signal at 21.4 MHz is present at A2A1E1.

4.6.7.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information in this paragraph corresponds to Table 4-21, Wideband IF Amplifier Fault Isolation Table. This chart is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure in paragraph 4.6.7.1.

2. Using an RF voltmeter RF probe tip, check each test point listed in Table 4-12. Where indicated, observe special instructions in the comments column.

3. When a faulty signal is encountered, replace the key component indicated in Table 4-21. Paragraph 4.6.9, Parts Replacement Guide, should be referred to as an aid in removing and replacing any PCB components.

4. Replacement of the indicated key components will normally restore the faulty test point signal to normal. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to Table 4-22, Wideband IF Amplifier Semiconductor Voltage Table, and Figure 6-8, Wideband IF Amplifier Schematic Diagram for additional aid in troubleshooting.

Table 4-21. Wideband IF Amplifier Fault Isolation Table

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
E1	58 mVrms at 21.4 MHz	Input cabling	Place 50 ohm terminators on rear panel A1J2 and A1J1
U1-2	145 mVrms	U1	
U2-2,4	90 mVrms	U2	

Table 4-22. Wideband IF Amplifier Semiconductor Voltage Table

DEVICE	PIN	VOLTAGE
U1	1	0 Vdc +5 Vdc

4.6.8 DIGITAL INTERFACE, A4, TESTING AND TROUBLESHOOTING

This paragraph describes the procedures to test, troubleshoot and repair the digital interface. An oscilloscope (see Table 4-3) is required to perform the tests outlined below.

4.6.8.1 Preliminary Setup Procedure

The following preliminary setup steps should be performed prior to testing or troubleshooting the digital interface:

1. Deenergize the demodulator

2. Remove the demodulator from the equipment frame (see paragraph 2.3.1 for details.)

3. Refer to paragraph 4.2 and use the procedure given to provide access to module A1A4.

4. Interconnect J1 on the demodulator rear panel with its mating connector on the equipment frame using the appropriate extender cable (see Figure 4-7.)

5. Energize the demodulator using the powerswitch on the equipment frame power supply. Set the demodulator front panel controls as follows:

a. LOCAL/REMOTE -- LOCAL
b. MAN/AGC -- MAN
c. IF GAIN -- Max. CW
d. DET. MODE -- AM
e. IF BW -- 4 MHz

4.6.8.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information in this paragraph corresponds to various fault isolation tables. These tables are used to isolate the digital interface module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedures in the sequence given. When a faulty signal is encountered, replace the key components indicated in the fault isolation table.

1. Perform the preliminary setup procedure in paragraph 4.6.8.1.

2. Using the oscilloscope, verify the external input signals to microcontroller U1 using the following Table 4-23.

Table 4-23. Microcontroller Input Signals

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
U1-pins 1-8,10	Pins 4 and 5 low. All others are high	Front Panel Switches	These signals are based on inputs given in paragraph 4.6.8.1
U1-12 (INT 0)	Logic high	U10, U14, U15 U16, U1	With controller disconnected. Pulse train (200 ms) will be seen with controller connected
U1-13 (INT 1)	Logic High	U1	With controller disconnected. Pulse train (200ms) will be seen with controller connected.
U1-18,19	10 MHz sine wave 5 V	Y1, U1	Clock signal
U1-9	0 Vdc	U1, C11	
U1-40	+5 Vdc	U20	

3. Using the oscilloscope, verify microcontroller U1 data bus and control signal activity using Table 4-24.

Table 4-24. Microcontroller Bus Activity Check

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
U1 pins 32-39 (AD0-AD7)	Rapidly changing logic levels on each pin	U1	Irregular pulse trains should be observed
U1 pins 21-24 (A8-A11)	Rapidly changing logic levels on each pin	U1	
U1-16 (WR)	Sharp, negative going pulse, 3 ms prr.	U1	
U1-29 (PSEN)	Square wave, .5 us prr.	U1	
U1-30 (ALE)	Square wave, .4 us prr.	U1	
U1-11 (REM)	High	U1	

4. Using the oscilloscope, verify I/O signal activity using Table 4-25.

Table 4-25. Digital Interface I/O Signal Check

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMPONENT
U2 Q0-Q7 outputs	Rapidly changing logic levels on each pin	U2	Address decoder EN
U8-4	Sharp, negative going pulse, 3 ms. prr.	U14	
U8-14 (Y1)	Sharp negative going pulse, 250 us. prr.	U8	
U8-13 (Y2)	Sharp, negative going pulses, 250 us. prr.	U8	
U8-12 (Y3)	Four, negative going pulses on power up.	U8	

Table 4-25. Digital Interface I/O Signal Check (Cont'd)

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
U8-11 (Y4)	Sharp, negative going pulse 3ms. prr.	U8	
U8-7 (Y7)	Logic High	U8	
U5-2 (Q0)	Logic High	U5	
U5-5 (Q1)	Logic High	U5	
U5-6 (Q2)	Logic High	U5	
U5-9 (Q3)	Logic Low	U5	
U5-12 (Q4)	Logic Low	U5	
U5-15 (Q5)	Logic Low	U5	
U5-16 (Q6)	Logic High	U5	
U5-18 (Q7)	Logic Low	U5	
U6-6	Square wave, .6 us prr	U2, U1	
U6-4,18	+2.5 V	U17	D/A Reference
U7-8, 14	0 V	U7	These outputs vary only in REM mode with controller connected and active

5. Using the oscilloscope, check the serial data input and output lines of serial interface U12 and U13 using Table 4-26. Not that signals are provided in both LOCAL and REMOTE MODES.

Table 4-26. Serial Interface Data Check

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
U13-9	Sharp positive going pulse, 250 us prr.	U16	
U13-3	Low * Serial Pulse Train **	U13	Data Out Signal

Table 4-26. Serial Interface Data Check (Cont'd)

TEST POINT	NORMAL SIGNAL	KEY COMPONENTS	COMMENTS
U12-15	Sharp positive going pulse, 250 us prr.	U16	
U12-2	Low * Serial Pulse Train **	U14	

* Controller disconnected, LOCAL mode
** Controller connected, REM mode

6. The bandwidth ID bits can be checked by connecting an oscilloscope to inputs of U4 pin 2,4,6,8 and 11 and selecting each bandwidth from the front panel.

	4	3	2	1	0
BW-1 - 150 kHz -	0	0	1	1	1
BW2 - 500 kHz -	1	0	1	0	0
BW3 - 1 MHz -	1	0	1	0	1
BW4 - 4 MHz -	1	0	1	1	1

7. Replacement of key components indicated in the tables provided in this test procedure for the digital interface module will normally restore the faulty test point signal to normal. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary.

4.6.9 PARTS REPLACEMENT GUIDELINES

This paragraph provides techniques to assist the technician in replacing components on PC boards.

WARNING

To prevent electrical shock or damage to the receiver, always disconnect the receiver from the ac power source before soldering or replacing components.

4.6.9.1 Soldering Techniques

When removing components from a printed circuit board for inspection or replacement, be especially careful not to damage the track. The soldering iron power should be no larger than 40 W, and a solder sipper or wicking procedure should be employed when removing solder. Use non-corrosive soldering flux when removing solder by wicking. When returning components to the board, make sure that holes are clear and that leads do not catch the edge edge of the track and lift it from the board. Use a good grade of rosin core

60/40 solder. Apply heat no longer than is necessary to achieve a good joint. Use a heat sink where possible.

4.6.9.2 Component Replacement

Specific guidelines for replacing the various kinds of components are as follows:

1. When soldering or unsoldering diodes or resistors, solder quickly to allow as little heat conduction as possible. When wiring permits, use a heat sink between the soldering iron and the part.

2. When soldering or unsoldering transistors, use a low wattage iron and a heat sink. Solder as quickly as possible. The use of a circular soldering tip to heat all three or four joings simultaneously is recommended.

3. When soldering or unsoldering glass or ceramic capacitors, use a heat sink between the capacitor and the iron. Excessive heat will crack the capacitor body.

4. When any electronic part is removed, note the position of the part and its leads, and replace it the same way.

4.6.9.3 Realignment

Replacement of semiconductors or tuned circuit components may affect the alignment of the PC board. Realignment may be necessary to return the PC board to normal operation.

4.7 DEMODULATOR ALIGNMENT PROCEDURES

4.7.1 GENERAL

The following Alignment procedures should be performed only when indicated by the result of Performance Testing (paragraph 4.4) or Troubleshooting (paragraph 4.5). Prior to performing any alignment, be sure to allow 30 minutes for test equipment warm-up.

4.7.2 IF Gain Adjustment

1. Refer to paragraph 4.2 and use the procedure given to gain access to module A1A2.

2. Connect demodulator as shown in Figure 4-8

3. Using the front panel controls, set the demodulator to the following parameters:

   a. Bandwidth - 150 kHz
   b. Gain Control - Manual
   c. IF Gain Control - Maximum Clockwise
   d. Detection Mode - AM

4. Set the signal generator output frequency to 21.400 MHz, unmodulated, and set the output level to -88 dBm.

5. Set RF voltmeter to -20 dBm range.

6. Adjust attenuator A1A2AT1 to obtain an indication of -20 dBm +/- 2dB on RF voltmeter.

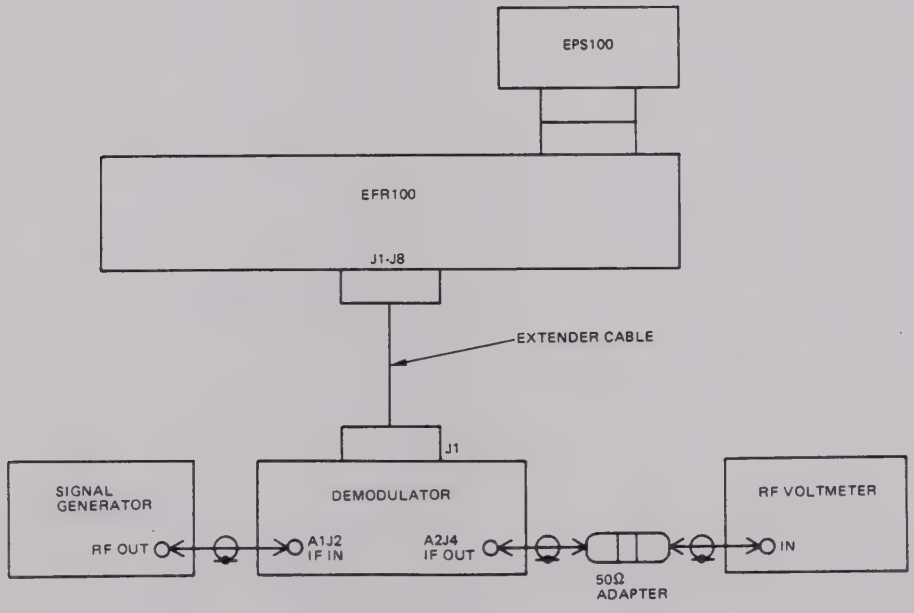


Figure 4-8. IF Gain Adjustment Equipment Setup

4.7.3 VIDEO OUTPUT OFFSET ADJUSTMENT

1. Refer to paragraph 4.2 and use the procedure given to gain access to module A1A2.

2. Connect demodulator as shown in Figure 4-9.

3. Using the front panel controls, set the demodulator to the following parameters:

   a. Bandwidth - 150 kHz
   b. Gain Control - Manual
   c. IF Gain Control - Maximum clockwise
   d. Detection Mode - AM

4. Set the digital multimeter to 2 Vdc rage.

5. Adjust variable resistor A1A2R34 to obtain an indication of 0 Vdc +/-.05 Vdc on multimeter.

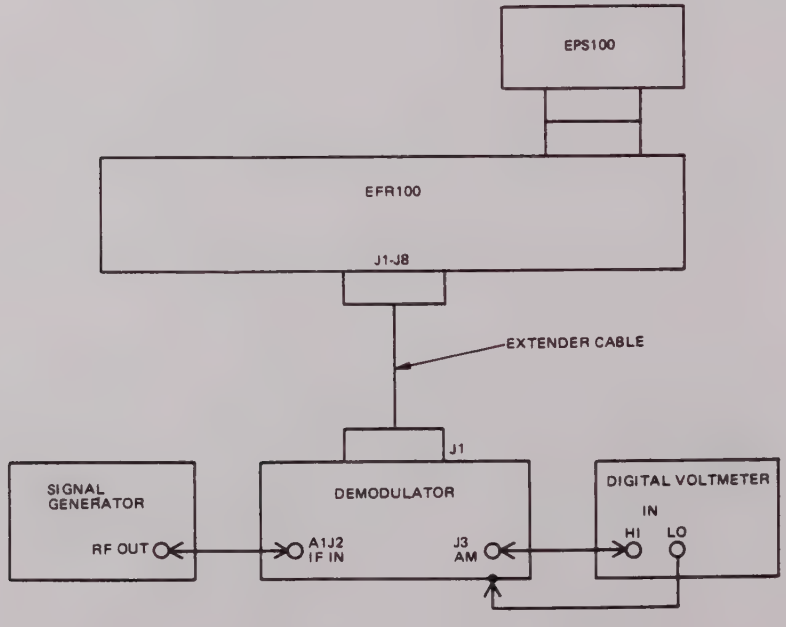


Figure 4-9. Video Output Offset Adjustment Equipment Setup

4.7.4 AM VIDEO LEVEL ADJUSTMENT

1. Refer to paragraph 4.2 and use the procedure given to gain access to module A1A3.

2. Connect demodulator as shown in Figure 4-10.

3. Using the front panel controls, set the demodulator to the following parameters:

   a. Bandwidth - 150 kHz
   b. Gain Control - AGC
   c. Detection Mode - AM

4. Set the signal generator output frequency to 21.400 MHz, AM, and set 50% modulation at 400 Hz rate.

5. Set oscilloscope settings to .5V/DIV Vertical and 5 msec Hor. Time Base.

6. Adjust variable resister A1A3R11 to obtain an indication on oscilloscope of 1 Vpp.

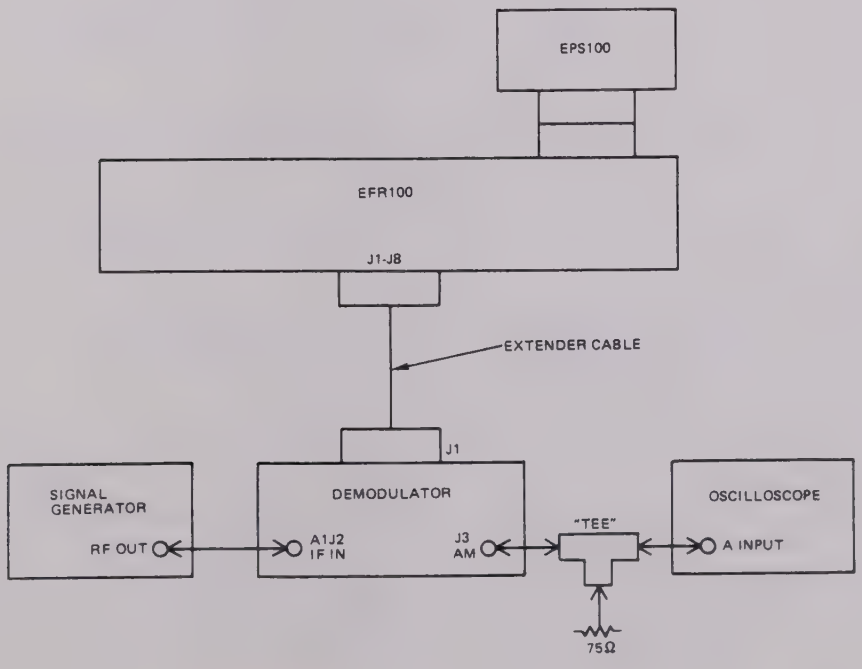


Figure 4-10. AM Video Level Adjustment Equipment Setup

4.7.5 FM DETECTOR ALIGNMENT

1. Refer to paragraph 4.2 and use the procedure given to gain access to module A1A5.

2. Connect demodulator as shown in Figure 4-11.

3. Using the front panel controls, set the demodulator to the following parameters:

   a. Bandwidth - 150 kHz
   b. Gain Control - AGC
   c. Detection Mode - FM

4. Set the sweep generator setting to a center frequency output of 21.4 MHz, sweep width to 500 kHz, and output level to -74 dBm.

5. Set oscilloscope settings to .5V/DIV vertical and Ext. Input Hor.

6. Set the digital multimeter to the 2 Vdc range.

7. Adjust A1A5A1C6 to obtain an indication on the oscilloscope as shown in Figure 4-12.

8. Set the demodulator bandwidth to 500 kHz.

9. Turn off sweep generator. Connect jumper from A1A5P4 to ground.

10. Adjust offset potentiometer A1A5A2R8 to obtain an indication on the digital multimeter of 0 Vdc +/-.05 Vdc. Remove jumper.

11. Turn on sweep generator and set sweep width to 1.5 MHz.

12. Adjust A1A5A2C6 and A1A5A2C9 to obtain an indication on the oscilloscope as shown in Figure 4-12.

13. Set the demodulator bandwidth to 1 MHz.

14. Turn off sweep generator. Connect jumper from A1A5P4 to ground.

15. Adjust offset potentiometer A1A5A3R8 to obtain an indication on the digital multimeter of 0 Vdc +/-.05 Vdc.

16. Turn on sweep generator and set sweep width to 3 MHz.

17. Adjust A1A5A3C6 and A1A5A3C9 to obtain an indication on the oscilloscope as shown in Figure 4-12.

18. Set the demodulator bandwidth to 4 MHz.

19. Turn off sweep generator. Connect jumper from A1A5P4 to ground.

20. Adjust offset potentiometer A1A5A4R8 to obtain an indication on the digital multimeter of 0 Vdc +/-.05 Vdc. Remove jumper.

21. Turn on sweep generator and set sweep width to 10 MHz.

22. Adjust A1A5A4C6 and A1A5A4C9 to obtain an indication on the oscilloscope as shown in Figure 4-12.

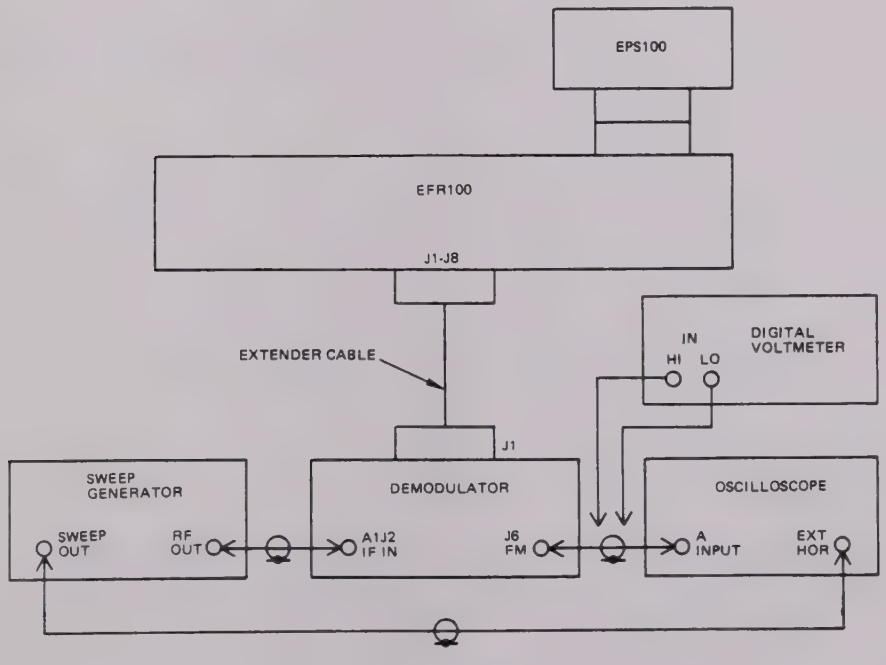


Figure 4-11. FM Detector Alignment Equipment Setup

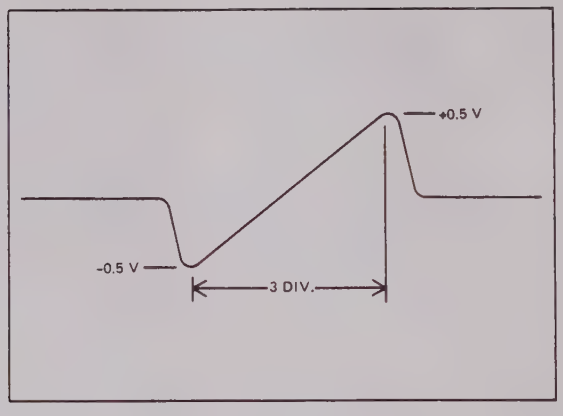


Figure 4-12. FM Detector Alignment Oscilloscope Indication

4.7.6 FM VIDEO LEVEL ADJUSTMENT

1. Refer to paragraph 4.2 and use the procedure given to gain access to module A1A5.

2. Connect demodulator as shown in Figure 4-13.

3. Using the front panel controls, set the demodulator to the following parameters:

   a. Bandwidth - 150 kHz
   b. Gain Control - AGC
   c. Detection Mode - AM

4. Set the signal generator output frequency to 21.400 MHz, FM modulation to 400 Hz, output level to -74 dBm, and deviation to 50 kHz.

5. Set oscilloscope settings to .5V/DIV Vertical and 5 msec Hor. Time Base.

6. Adjust variable resister A1A5A1R13 to obtain an indication of 0.6 Vpp on oscilloscope.

7. Set demodulator bandwidth to 500 kHz.

8. Set signal generator FM deviation to 150 kHz.

9. Adjust variable resister A1A5A2R7 to obtain an indication of 0.6 Vpp on oscilloscope.

10. Set demodulator bandwidth to 1 MHz.

11. Set signal generator FM deviation to 300 kHz.

12. Adjust variable resistor A1A5A3R7 to obtain an indication of 0.6 Vpp on oscilloscope.

13. Set demodulator bandwidth to 4 MHz.

14. Set signal generator FM deviation to 1.3 MHz.

15. Adjust variable resistor A1A5A4R7 to obtain an indication of 0.6 Vpp on oscilloscope.

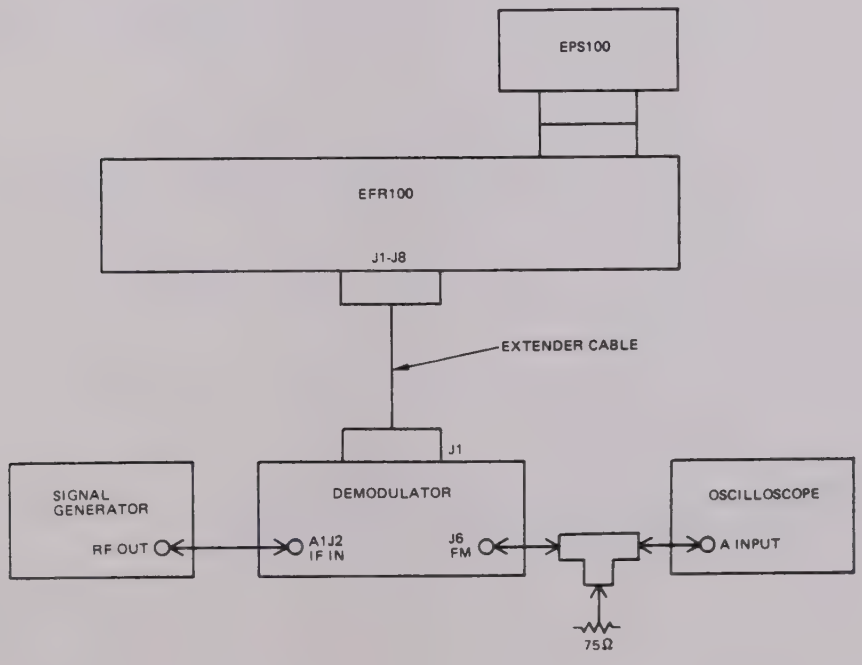


Figure 4-13. FM Video Level Adjustment Equipment Setup

4.7.7 WB/NB FILTER ALIGNMENT

1. Refer to paragraph 4.2 and use the procedure given to gain access to module A1A2.

2. Connect demodulator as shown in Figure 4-14

3. Using the front panel controls, set the demodulator to the following parameters:

   a. Bandwidth - 150 kHz
   b. Gain Control - AGC
   c. Detection Mode - FM

4. Set sweep generator setting to a center frequency output of 21.4 MHz, sweep width to 10 MHz, and output level to -74 dBm.

5. Set oscilloscope settings to .5/DIV vertical and Ext. Input Hor.

6. Remove the 150 kHz bandpass filter and insert a jumper in its place.

7. Energize the dc power source.

8. With cover on the module, adjust A1A2C22 and C25 for a symetrical response of approximately 400 kHz bandwidth.

9. Deenergize the dc power source.

10. Replace the 150 kHz bandpass filter. Remove the 4 MHz bandpass filter and insert a jumper in its place.

11. Energize the dc power source. Select 4 MHz BW position.

12. Adjust A1A2C1, C8, and C10 for a symetrical broad band response.

13. Deenergize the dc power source.

14. Replace the 4 MHz bandpass filter.

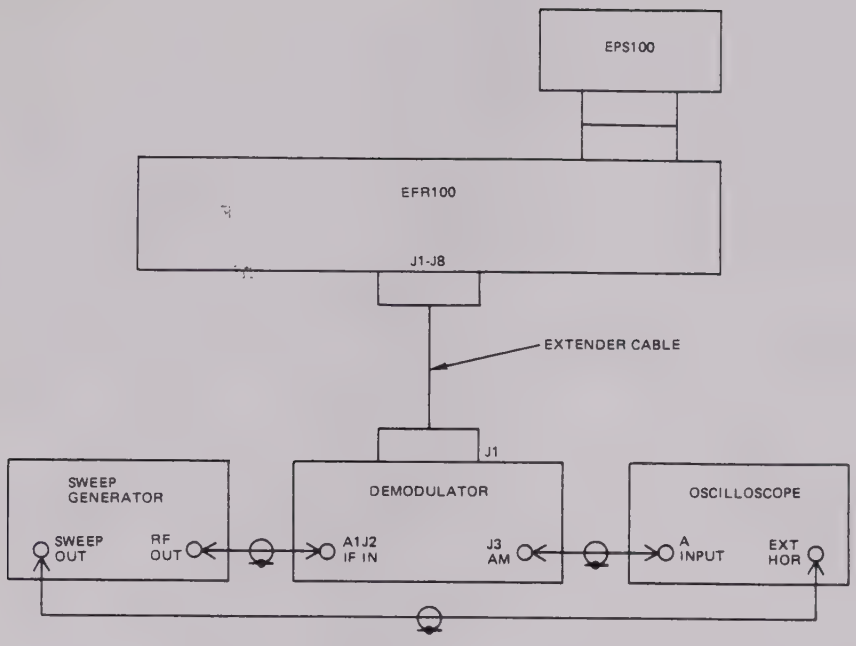


Figure 4-14. WB/NB Filter Alignment Equipment Setup

SECTION V

REPLACEMENT PARTS LIST

5.1 UNIT NUMBERING METHOD

The unit numbering method of assigning reference designations (electrical symbol numbers) has been used to identify assemblies, subassemblies (and modules) and parts. An example of the unit numbering method follows:

Subassembly Designation A1	R1 Class and No. of Item
Identify from right to left as:	First (1) resistor (R) of first (1) subassembly (A)

As shown on the main chassis schematic, components which are an integral part of the main chassis have no subassembly designation.

5.2 REFERENCE DESIGNATION PREFIX

Partial reference designations have been used on the equipment and on the illustrations in this manual. The partial reference designations consist of the class letter(s) and identifying item number. The complete reference designations may be obtained by placing the proper prefix before the partial reference designations. Reference Designation Prefixes are provided on drawings and illustrations in parentheses within the figure titles.

5.3 LIST OF MANUFACTURERS

Mfr. Code	Name and Address
00779	AMP, Incorporated P.O. Box 3608 Harrisburg, PA 17105
01121	Allen-Bradley Company 1201 South 2nd Street Milwaukee, WI 53204
01295	Texas Instruments, Inc. Semiconductor-Components Div. 15300 North Central Expressway Dallas, TX 75231
02735	RCA Corporation Solid State Division Route 202 Somerville, NJ 08876
04013	Taurus Corporation 1 Academy Hill Lambertville, NJ 08530
04713	Motorola Incorporated Semiconductor Products Div. 5005 East McDowell Road Phoenix, AZ 85008

Mfr. Code	Name and Address
06090	Raychem Corporation 300 Constitution Drive Menlo Park, CA 94025
06776	Robinson Nugent Inc. 800 E. 8th Street P.O. Box 1208 New Albany, IN 47150
08717	The Sloan Co. 7704 San Fernando Rd. Sun Valley, CA 91353
09021	Airco, Inc. Airco Electronics Bradford, PA 17055
14193	CAL-R Inc. 1601 Olympic Blvd. P.O. Box 1397 Santa Monica, CA 90406
14632	Watkins-Johnson Company 700 Quince Orchard Road Gaithersburg, MD 20878
15542	Mini-Circuits Laboratory Division of Scientific Components Corp. 2625 E. 14th Street Brooklyn, NY 11235
17856	Siliconix, Inc. 2201 Laurelwood Road Santa Clara, CA 95050
18324	Signetics Corporation 811 East Arques Avenue Sunnyvale, CA 94086
19505	Applied Eng. Products, Co. Division of Samarious, Inc. 300 Seymour Avenue Derby, CT 06418
22526	Du Pont EI De Nemours and Co. Inc. Photo Products Dept. Berg Electronics Div. Route 83 New Cumberland, PA 17070
24355	Analog Devices Inc. Rt. 1 Industrial Park P.O. Box 280 Norwood, MA 02062
27014	National Semi-Conductor Corp. 2950 San Ysidro Way Santa Clara, CA 95051
27956	Relcom 3333 Hillview Avenue Palo Alto, CA 94304
28480	Hewlett-Packard Company Corporate Headquarters 1501 Page Mill Road Palo Alto, CA 94304
34649	Intel Corporation 3065 Bowers Ave. Santa Clara, CA 95051
51642	Centre Engineering Inc. 2820 E. College Ave. State College, PA 16801
52648	Plessey Trading Corporation 1641 Kaiser Ave. Irvine, CA 92714

Mfr. Code	Name and Address
54473	Matsushita Electric Corp. of America One Panasonic Way P.O. Box 1501 Secaucus, NJ 07094
55027	Q-Bit Corporation 2575 Pacific Ave. NE Palm Bay, FL 32904
55322	Samtec Inc. 810 Progress Blvd. P.O. Box 1147 New Albany, IN 41750
56289	Sprague Electric Company Marshall Street North Adams, MA 01247
71279	Cambridge Thermionic Corp. 445 Concord Avenue Cambridge, MA 02138
71468	ITT Cannon Electric 10550 Talbert Ave. P.O. Box 8040 Fountain Valley, CA 92708
73138	Beckman Instruments, Inc. Helipot Division 2500 Harbor Boulevard Fullerton, CA 92634
80058	Joint Electronic Type Designation System
80131	Electronic Industries Assoc. 2001 Eye Street, NW Washington, DC 20006
80294	Bourns Instruments Inc. 6135 Magnolia Ave. Riverside, CA 92506
81312	Winchester Electronics Division of Litton Ind. Oakville, CT 06779
81349	Military Specifications
84048	Vernitron Corp. VRN International Div. 2801 72nd St. North P.O. Box 44000 St. Petersburg, FL 33743
95121	Quality Components, Inc. P.O. Box 113 St. Mary's, PA 15857
95146	ALCO Electronic Products Inc. 1551 Osgood Street North Andover, MA 01845
99800	American Precision Industries Delevan Electronics Division 270 Quaker Road East Aurora, NY 14052

5.4 PARTS LIST

The parts list which follows contains all electrical parts used in the equipment and certain mechanical parts which are subject to unusual wear or damage. When ordering replacement parts from Watkins-Johnson Company, specify the type and serial number of the equipment and the reference designation and description of each part ordered. The list of manufacturers provided in paragraph 5.3 and the manufacturer's part number for components are included as a guide to the user of the equipment in the field. These parts may not necessarily agree with the parts installed in the equipment; however, the parts specified in this list will provide satisfactory operation of the equipment. Replacement parts may be obtained from any manufacturer as long as the physical and electrical parameters of the part selected agree with the original indicated part. In the case of components defined by a military or industrial specification, a vendor which can provide the necessary component is suggested as a convenience to the user.

NOTE

As improved semi-conductors become available, it is the policy of Watkins-Johnson to incorporate them in proprietary products. For this reason some transistors, diodes, and integrated circuits installed in the equipment may not agree with those specified in the parts list and schematic diagrams of this manual. However, the semi-conductors designated in the manual may be substituted in every case with satisfactory results.

5.5 TYPE WJ-9040 IFD121 IF DEMODULATOR, MAIN CHASSIS

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	IF Demodulator Assembly	1	794465-1	14632	
A2	Wideband Amplifier Assembly	1	794466-1	14632	
DS1	Lamp/LED (Part of XDS1)	-	4RO	08717	
MP1	Handle	1	10221-B-0632-4A	06540	
MP2	Knob	1	PS50D1/BLK	21604	
MP3	Knob	2	PS50PL1/BLK	21604	
MP4	Same as MP3				
MP5	Screw, Retainer	4	6251D-SS-0632	06540	
MP6 Thru MP8	Same as MP5				
P1	Plug Assembly	1	271420-1	14632	
R1	Resistor, Variable, Composition: 10 k, 10%, 1 W	1	70A3N048L103U	01121	
S1	Switch, Toggle	2	MTA106D	95146	
S2	Same as S1				
S3	Switch, Rotary	2	MR5-1-12	95146	
S4	Same as S3				
W1	Cable Assembly	1	17300-351-1	14632	
W1P1	Connector, Plug, SMB	2	2002-1551-005	19505	
W1P2	Same as W1P1				
XDS1	Lamp Assembly, LED	1	122B-RL-QB-4RO	08717	

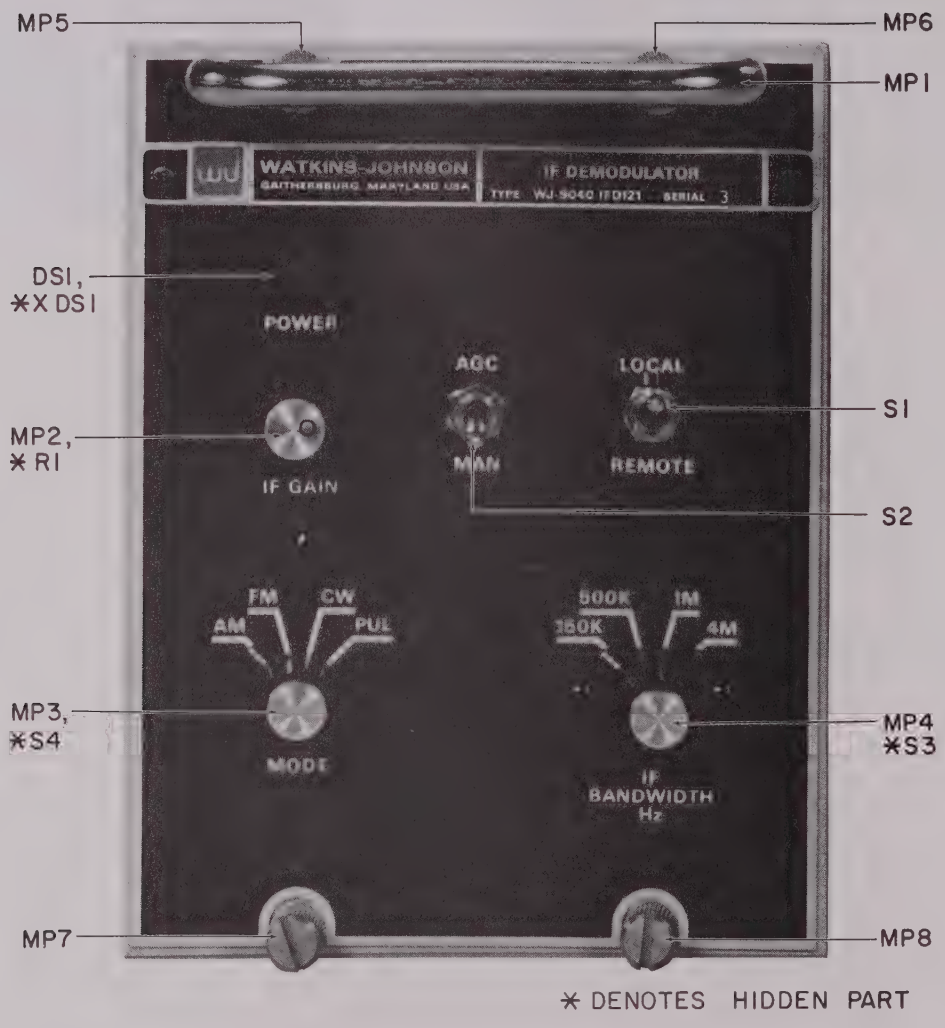


Figure 5-1. WJ-9040 IFD121 IF Demodulator,
Front Panel, Location of Components

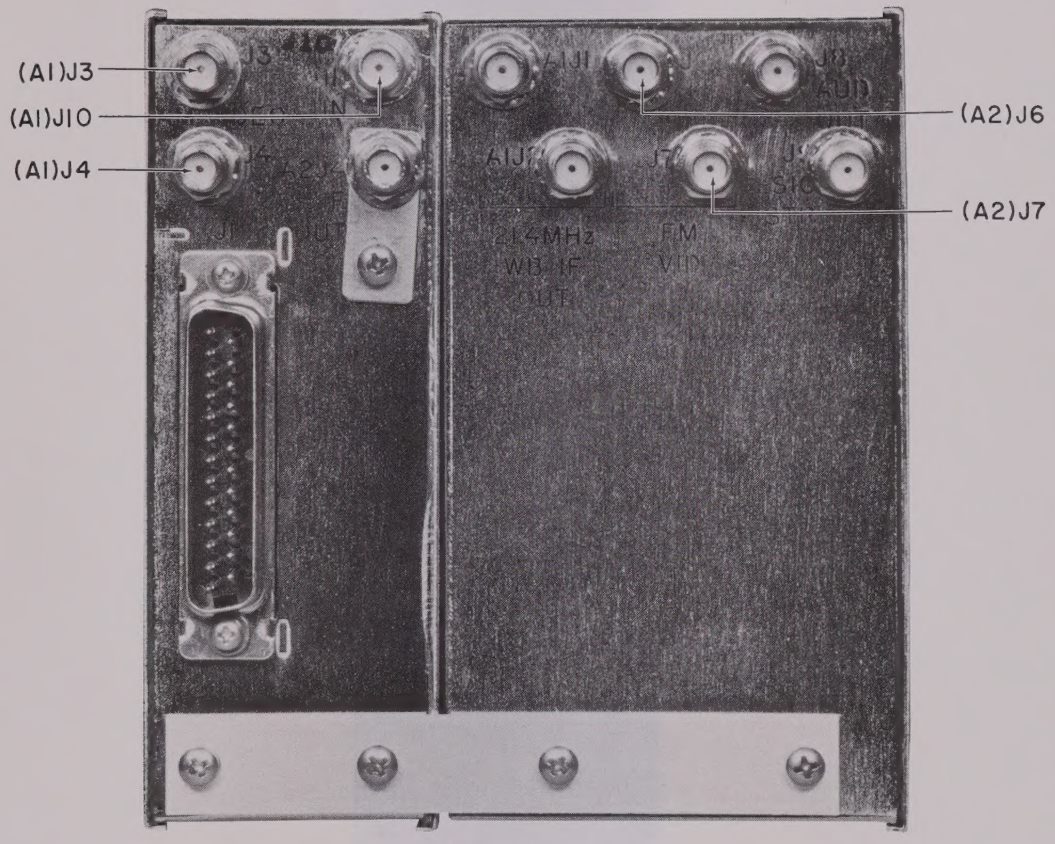


Figure 5-2. WJ-9040 IFD121 IF Demodulator,
Rear Panel, Location of Components

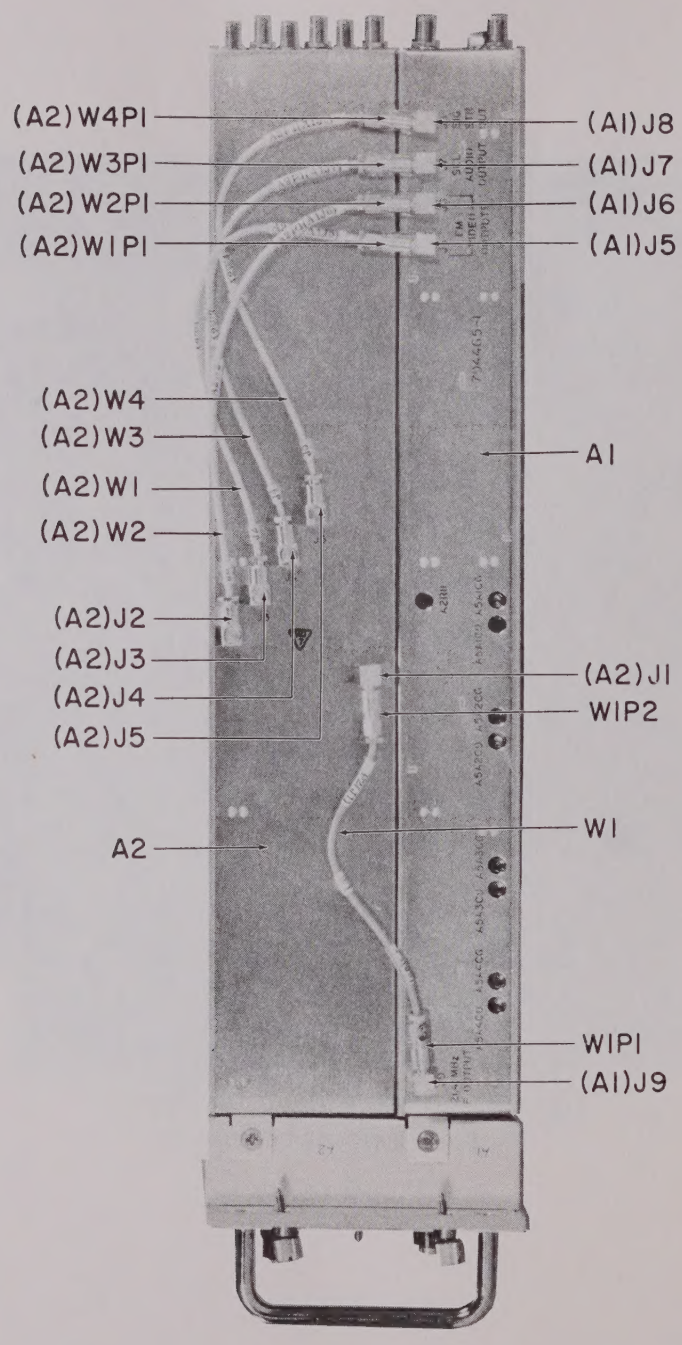


Figure 5-3. WJ-9040 IFD121 IF Demodulator,
Top View, Location of Components

MP MASTER
MA34478